

AKAI





SERVICE MANUAL

Model: LCT3285TA

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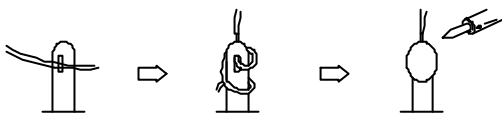
.....
This manual is the latest at the time of printing, and does not
include the modification which may be made after the printing,
by the constant improvement of product.
.....

I. Safety Instructions

 <div>CAUTION RISK OF ELECTRIC SHOCK DO NOT OPEN</div>  <p>CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.</p>	 <p>The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated "dangerous voltage" within the product's enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.</p>
	 <p>The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.</p>

PRECAUTIONS DURING SERVICING

1. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements. Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
2. Use specified internal Wiring. Note especially:
 - 1) Wires covered with PVC tubing
 - 2) Double insulated wires
 - 3) High voltage leads
3. Use specified insulating materials for hazardous live parts. Note especially:
 - 1) Insulating Tape
 - 2) PVC tubing
 - 3) Spacers (insulating barriers)
 - 4) Insulating sheets for transistors
 - 5) Plastic screws for fixing micro switches
4. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



5. Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
6. Check if replaced wires do not contact sharply edged or pointed parts.
7. Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

Used batteries with the ISO symbol for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can. Please leave them at an appropriate depot.



WARNING:

Before servicing this TV receiver, read the X-RAY RADIATION PRECAUTION, SAFETY INSTRUCTION and PRODUCT SAFETY NOTICE.

X-RAY RADIATION PRECAUTION

1. Excessively high can produce potentially hazardous X-RAY RADIATION. To avoid such hazards, the high voltage must not exceed the specified limit. The normal value of the high voltage of this TV receiver is 27 KV at zero beam current (minimum brightness). The high voltage must not exceed 30 KV under any circumstances. Each time when a receiver requires servicing, the high voltage should be checked. The reading of the high voltage is recommended to be recorded as a part of the service record. It is important to use an accurate and reliable high voltage meter.
2. The only source of X-RAY RADIATION in this TV receiver is the picture tube. For continued X-RAY RADIATION protection, the replacement tube must be exactly the same type as specified in the parts list.
3. Some parts in this TV receiver have special safety related characteristics for X-RADIATION protection. For continued safety, the parts replacement should be under taken only after referring the PRODUCT SAFETY NOTICE.

SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this TV receiver. The following are the necessary instructions to be observed before servicing.

1. An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
2. Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
3. To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.

4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.
5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high temperature components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads, metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner.

Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15 μ F AC type capacitor, between a good earth ground (water pipe, conductor etc.,) and the exposed metallic parts, one at a time.


Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 μ F capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.

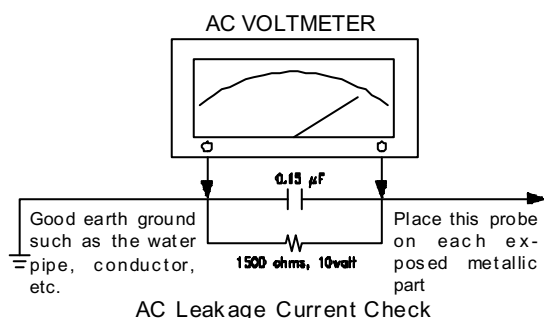
The measured voltage must not exceed 0.3V RMS.

This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.

The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this TV receiver have special safety-related characteristics. These characteristics are offer passed unnoticed by visual spection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc. The replacement parts which have these special safety characteristics are identified by  marks on the schematic diagram and on the parts list. Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, X-RAY RADIATION or other hazards.



1. Do not power on.

1.1 Please check AC cable if connect to AC plug.

Is true the connector don't connect to AC plug. Please connect it.

2.2 Please check AC cable if connect to AC power.

Is true the AC cable don't connect to AC power. Please connect it.

3.3 Please check power board of fuse if broken.

If the F1 fuse is broken, Please pull out the AC cable from AC power. Please check AC L power and AC N ground by multimeter, The read number is infinite, the fuse is broke. then look up power board if not burn out place. Is true it. Please change power board or be changed power board.

2. The power on switch of green extinguish.

2.1 The power of led(indicator light) is red light, To touch power on key when indicator light wink.

Is true that the power DC output have somewhere short circuit.

Please check connector J39,J31 .If not connector direction is wrong.

Or the mainboard somewhere of power short circuit.

3.The power is normal work ,but don't backlight.

3.1 The indicator light work normal (green light).

Please check Main board of transistor Q1&collect if not has +5v voltage.

Is true Q18 collect hasn't +5v ,To check Q18 if fail. Or to check Q18 of base if not low.

(Low is working, high don't work).

Please refer to attached sheet A circuit diagram.

3.2 Please check backlight of connector if not it direction is wrong or the connector of wire compositor direction is wrong.

3.3 To check connector panel of voltage is +24v. It's true .Then to check of the first pin if it have +5V voltage, It's true , than to check power board of +24v voltage ,It's true. The panel of backlight board is fail. The change panel of backlight board.

Please refer to attached sheet B Panel of datasheet.

4.The screen don't have picture But have backlight.

4.1 To check to panel of voltage ,To check main board of bead L69 and L57 connect if not OK.Then check the L69 and L57 of voltage is +12v(27 inch panel voltage is +5v, To check L68 and L56) . Next to check fuse F1 and connector J10 if not is +12v(27 inch panel voltage is +5v). If isn't please check power board of connector CON5 if has +12v(27 inch panel voltage is +5v).

4.2To check to main board +12 V voltage. To check to main board IC U35 of the first pin if

+5v voltage ,It's fail. It's low (close 0 v) working.

The circuit diagram follow down:

Please refer to attached sheet A circuit diagram.

5.The remote control don't be control.

6.1 The check batteries of remote control if it run out of .

6.2 To check main board of connector J21 of wire connect fastness and the connector of wire open.

Please refer to attached sheet A circuit diagram.

6.The sound don't output.

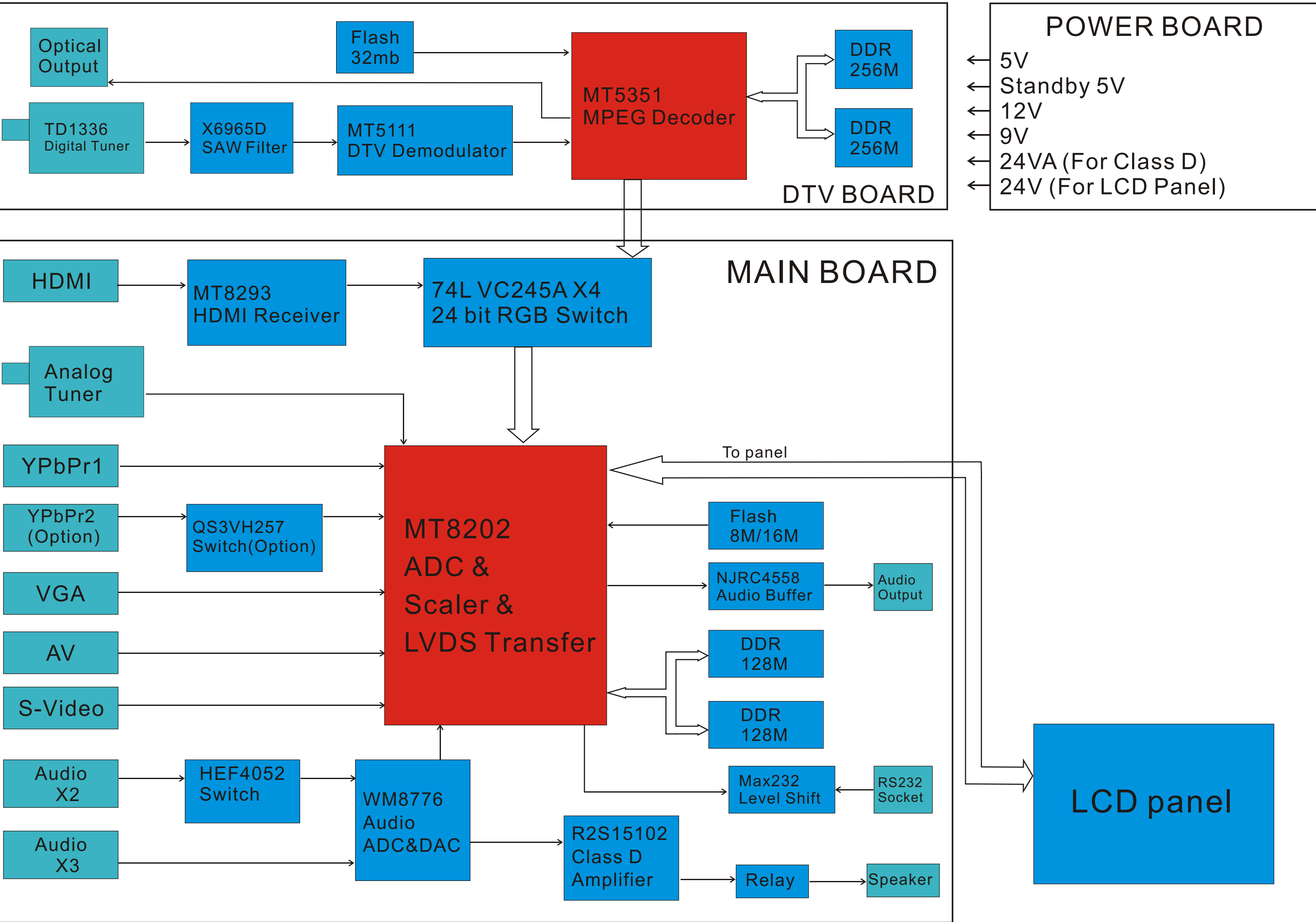
7.1 To check main board +24v voltage of connector J8 ,It's true not +24v voltage. Then to to check power main +24v fail .

Please refer to attached sheet A circuit diagram.

7.The DTV don't detect .

7.1 To check mainboard of connector J24 and DTV mainboard of connector HA1 of FCC wire if no connect fastness.

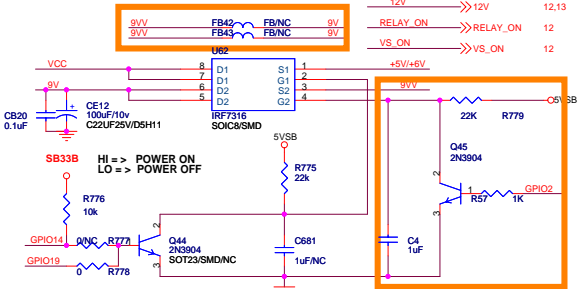
Please refer to attached sheet C of DTV circuit diagram.



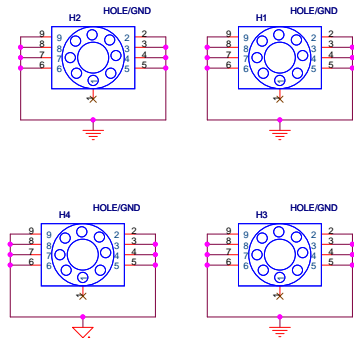
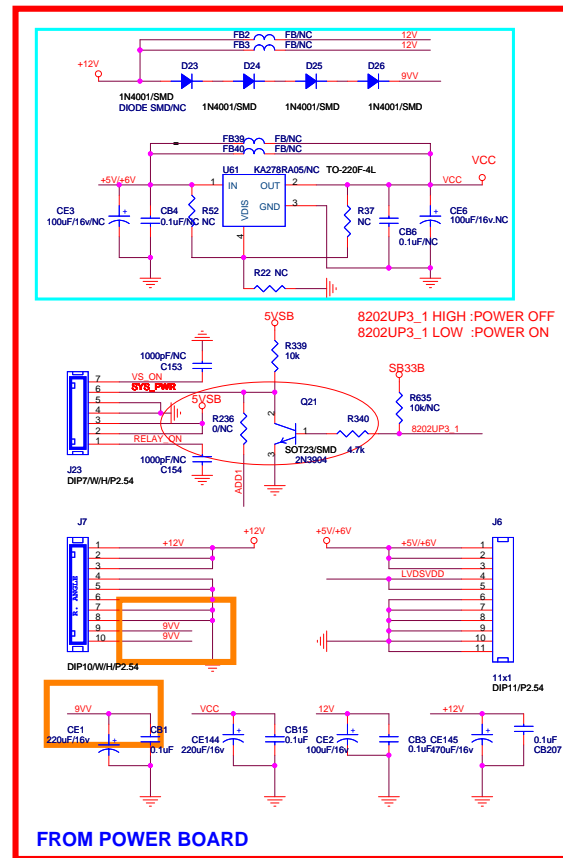
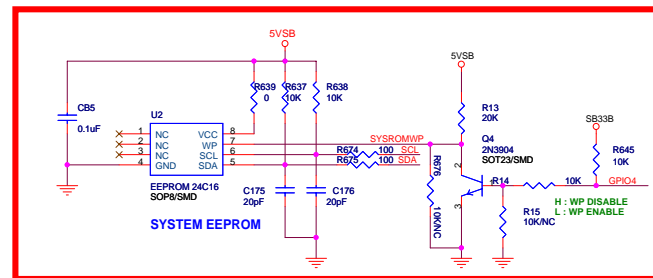
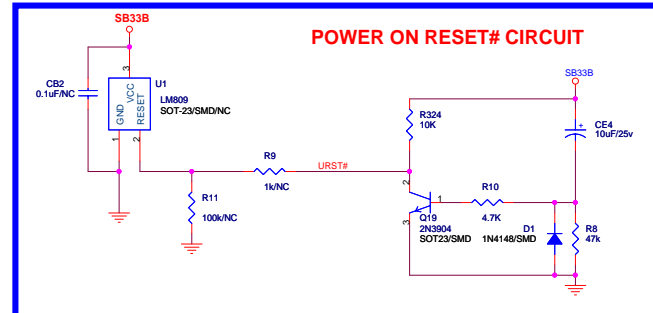
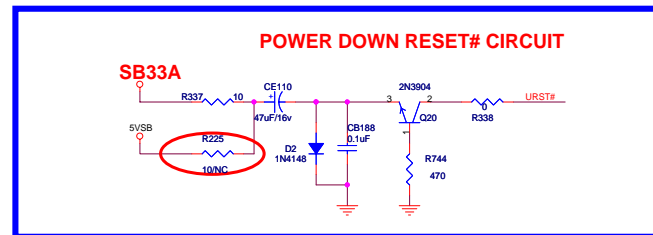
MT8202E (PBGA388) LCDTV BOARD 4 LAYERS FOR AKAI

1. INDEX / POWER / RESET / EEPROM
2. LDO
3. MT8202E PBGA388
4. MT8202 DECOUPLING
5. DDR MEMORY & FLASH
6. MT5351 INTERFACE
7. HDMI MT8293
8. DAUGHTER BOARD IN
9. WM8776 & VIDEO BYPASS
10. AUDIO / VIDEO IN CIRCUIT
11. VGA & PC AUDIO IN
12. LVDS OUT
13. BACK LIGHT / KEYPAD
14. TUNER IN
15. AV IN
16. AUDIO IN
17. AUDIO Amplifier

Rev	History	P#	Date
AKAI_MT8202_27US_LVDS_V0.0	New		2005/11/22
AKAI_MT8202_27US_HDMI_LVDS_V0.0	ADD HDMI / VIDEO / AUDIO CONNECTOR INPUT IN		

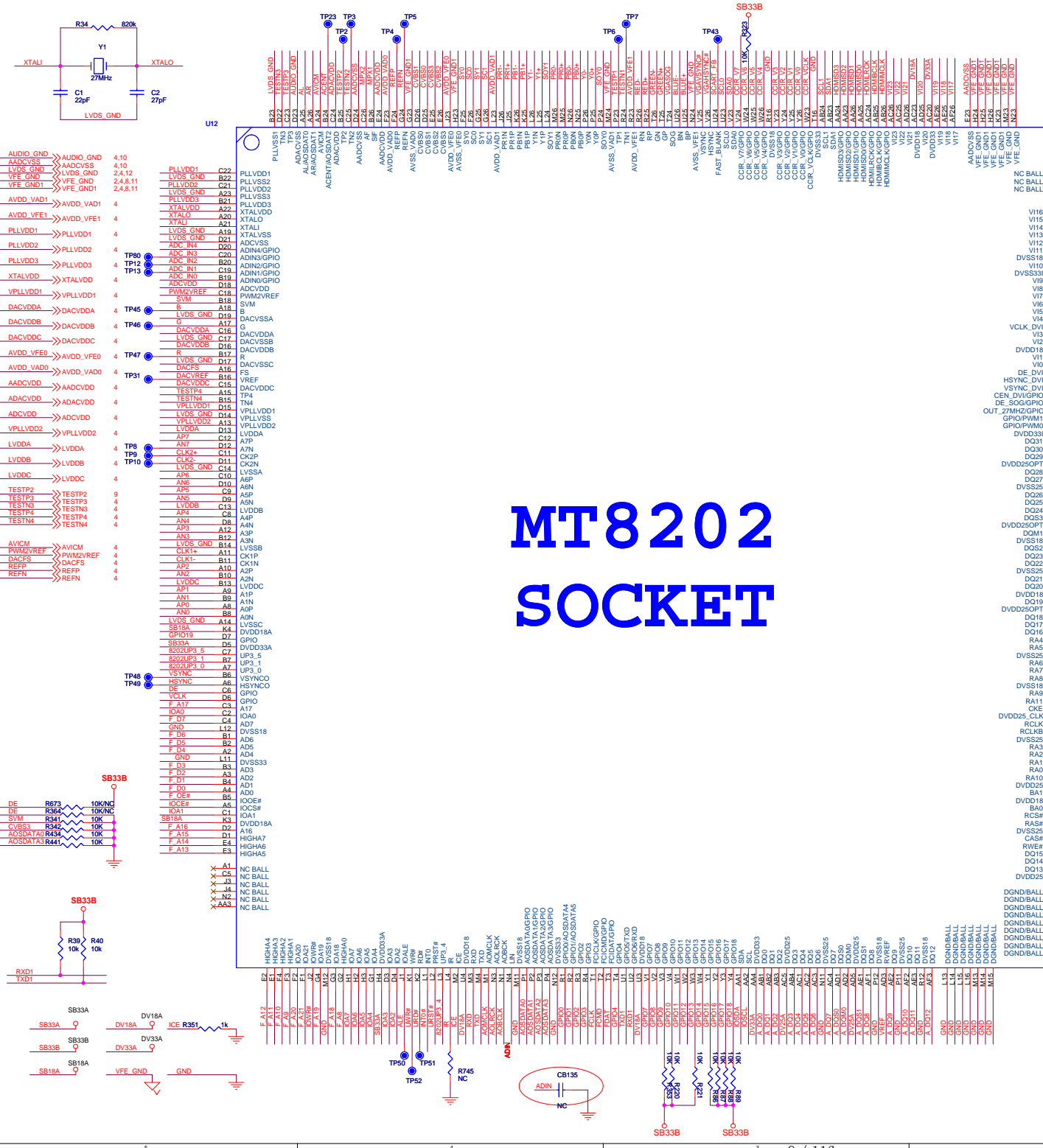


LVDSVDD	>>>LVDSGND	2,3,4
SCL	>>>SCL	9,14
SDA	>>>SDA	9,14
URST#	>>>URST#	3
8202UP3_1	>>>8202UP3_1	3
GPIO2	>>>GPIO2	3,12
GPIO4	>>>GPIO4	3
GPIO14	>>>GPIO14	3,13
GPIO19	>>>GPIO19	3,13
9V	>>>9V	7,9,14
12V	>>>12V	12,13
RELAY_ON	>>>RELAY_ON	12
VS_ON	>>>VS_ON	12



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Title			
INDEX / POWER / RESET / EEPROM			
Size	Document Number	AKAI_MT8202_27US_LVDS_V0.0	Rev 1
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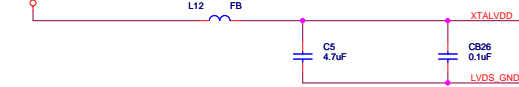


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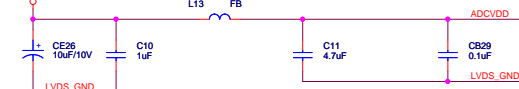
Title			
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C	AKAI_MT8202_27US_LVDS_V0.0	Checked	1
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STANDBY ANALOG POWER

ASB18A

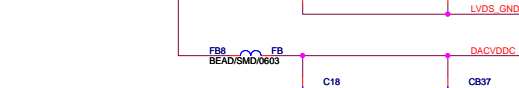
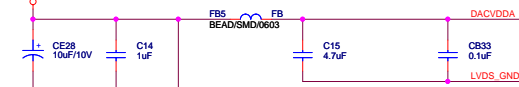


ASB33A



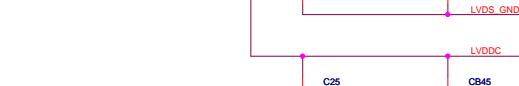
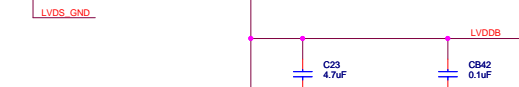
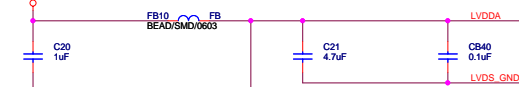
NORMAL VIDEO DAC POWER

DACVDD



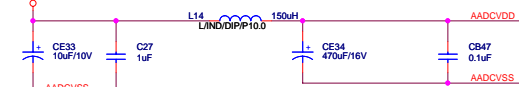
NORMAL VIDEO DAC POWER

AV33A



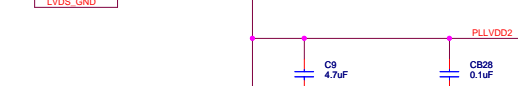
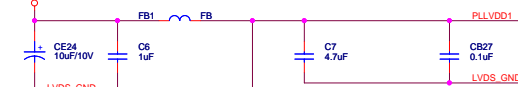
NORMAL AUDIO ADC / DAC POWER

ADC33A

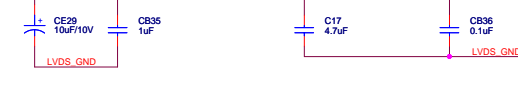
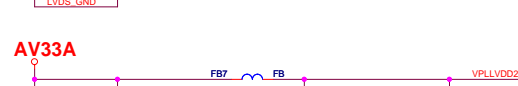
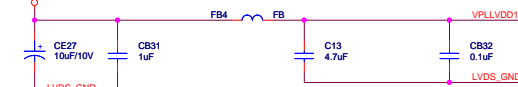


NORMAL ANALOG POWER

ASB18A

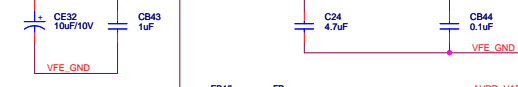
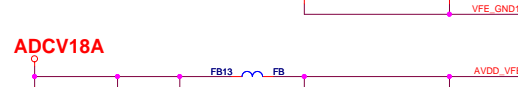
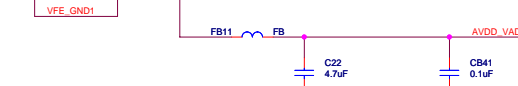
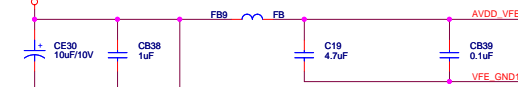


AV18A

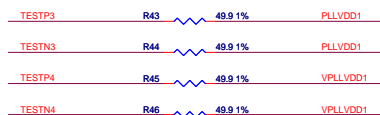
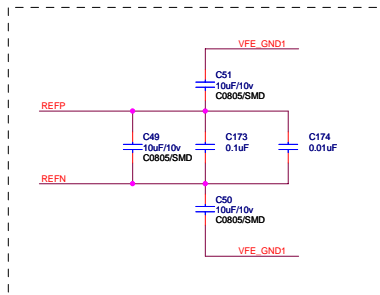


NORMAL VIDEO ADC POWER

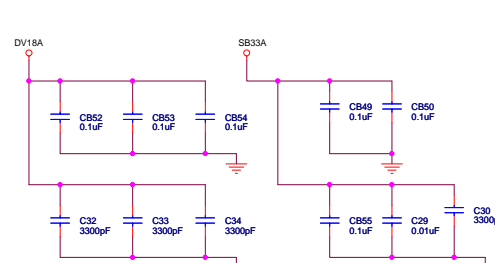
ADC33A



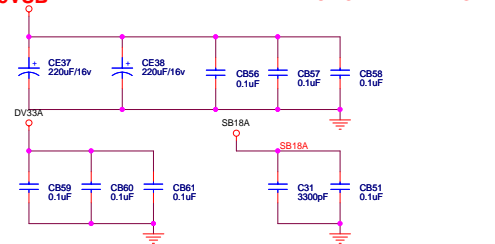
ADC18A



MT8202 DIGITAL POWER & DECOUPLING

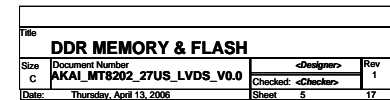


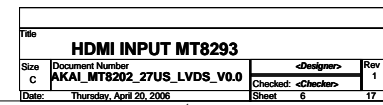
5VSB

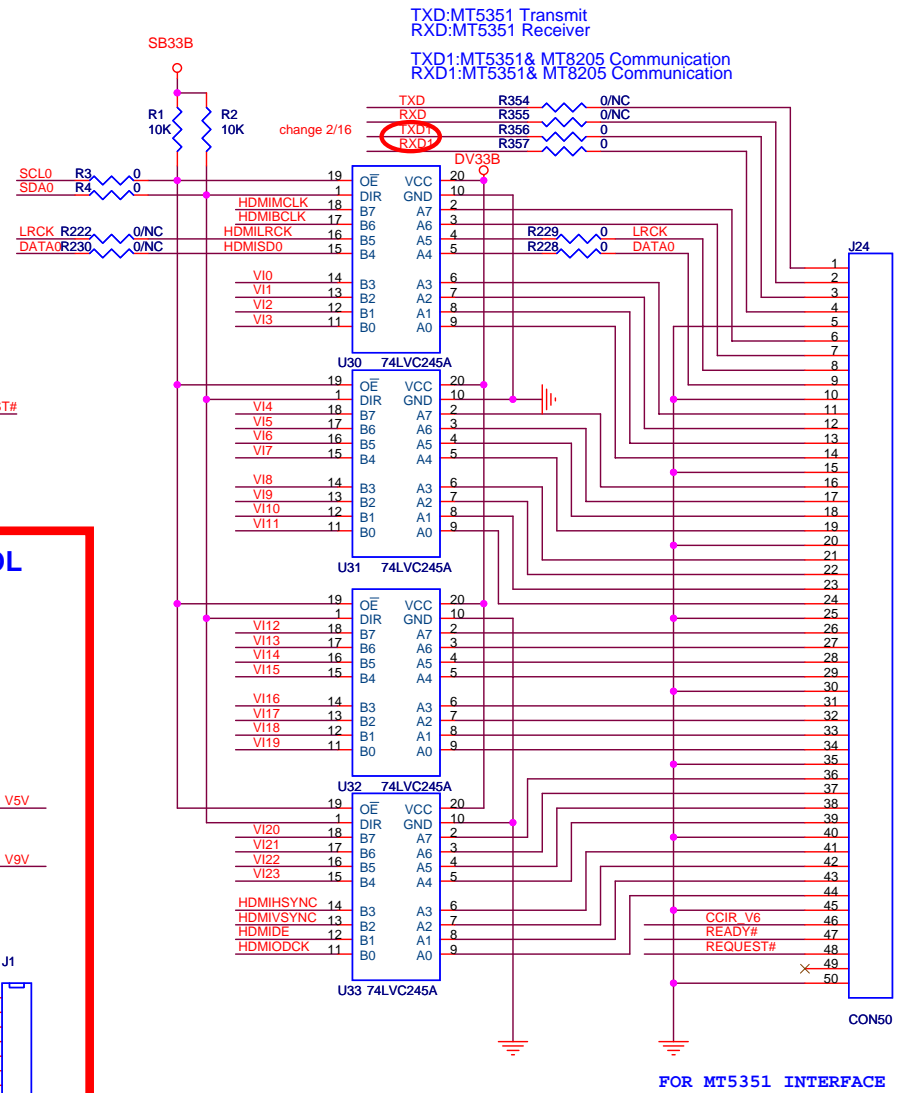
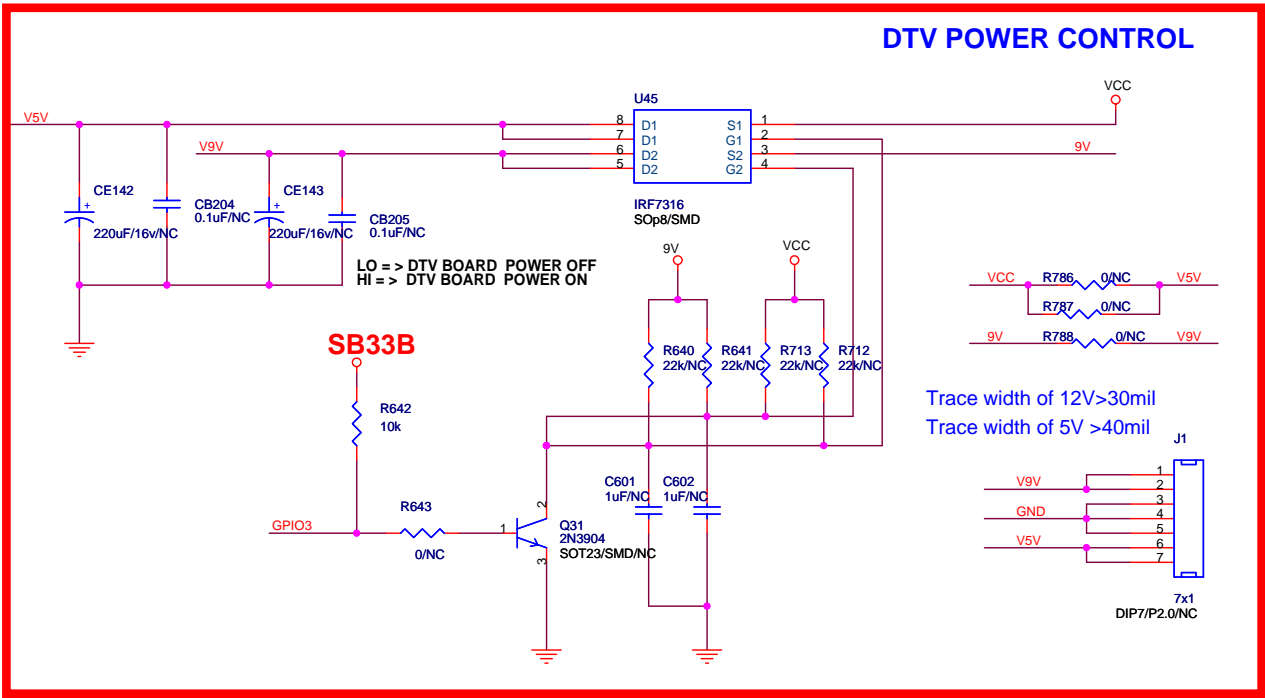
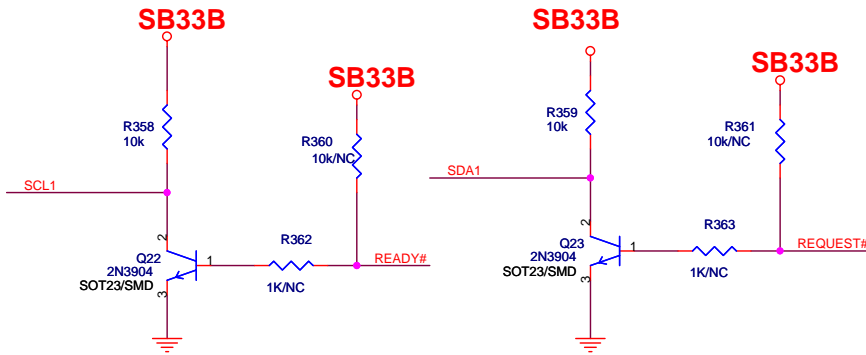
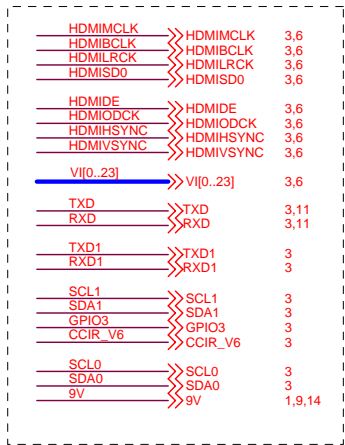


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File	MT8202 DECOUPLING	Designer	Rev
Size	Document Number	Checked	1
C	AKAI_MT8202_27US_LVDS_V0.0	Sheet	4
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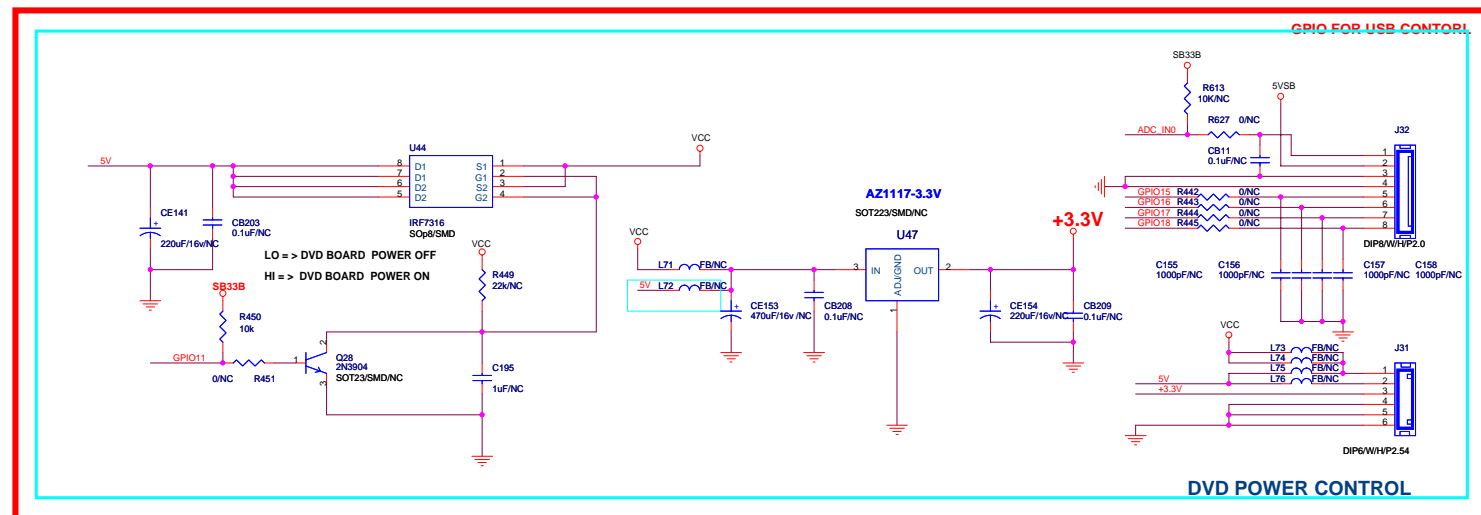
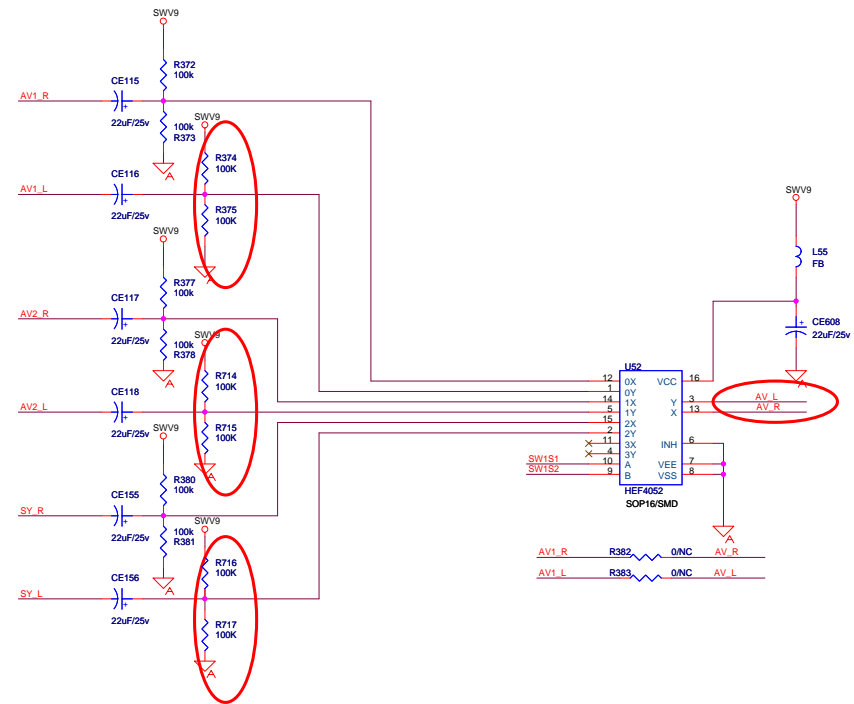
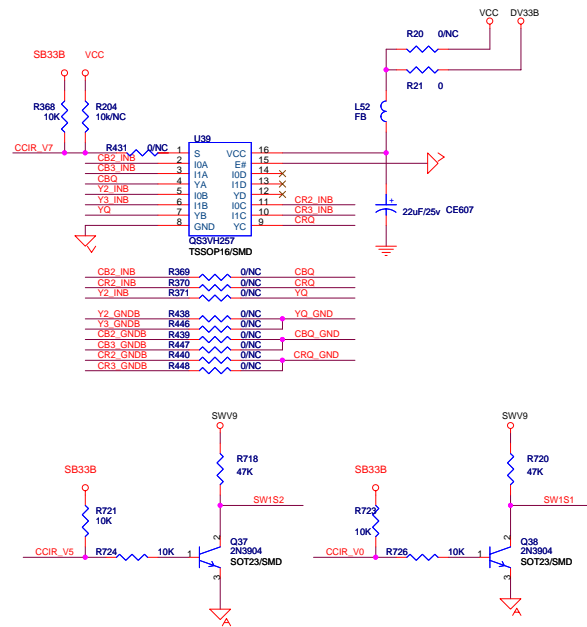
Title			
MT5351 INTERFACE			
Size	Document Number	Designer	Rev
B	AKAI_MT8202_27US_LVDS_V0.0	Checked: <Checker>	1
Date:	Thursday, April 13, 2006	Sheet	7

INPUT

ADC_IN0	ADC_IN0	3
CCIR_V0	CCIR_V0	3
CCIR_V5	CCIR_V5	3
CCIR_V7	CCIR_V7	3
GPIO11	GPIO11	3
GPIO15	GPIO15	3
GPIO16	GPIO16	3
GPIO17	GPIO17	3
GPIO18	GPIO18	3
VFE_GND	VFE_GND	2,3,4,11
AADC_VSS	AADC_VSS	3,4,10
AV1_R	AV1_R	15
AV1_L	AV1_L	15
AV2_R	AV2_R	15
AV2_L	AV2_L	15
SY_R	SY_R	15
SY_L	SY_L	15
Y2_INB	Y2_INB	15
Y2_GNDB	Y2_GNDB	15
Y2_GNDB	Y2_GNDB	10,15
CR2_INB	CR2_INB	15
CR2_GNDB	CR2_GNDB	10,15
Y3_INB	Y3_INB	15
Y3_GNDB	Y3_GNDB	15
Y3_GNDB	Y3_GNDB	10,15
CR3_INB	CR3_INB	15
CR3_GNDB	CR3_GNDB	15
CR3_GNDB	CR3_GNDB	10,15
9V	9V	1,7,9,14

OUTPUT

AV_R	AV_R	9
AV_L	AV_L	9
YQ	YQ	10
CBQ	CBQ	10
CRQ	CRQ	10
YQ_GND	YQ_GND	10
CBQ_GND	CBQ_GND	10
CRQ_GND	CRQ_GND	10



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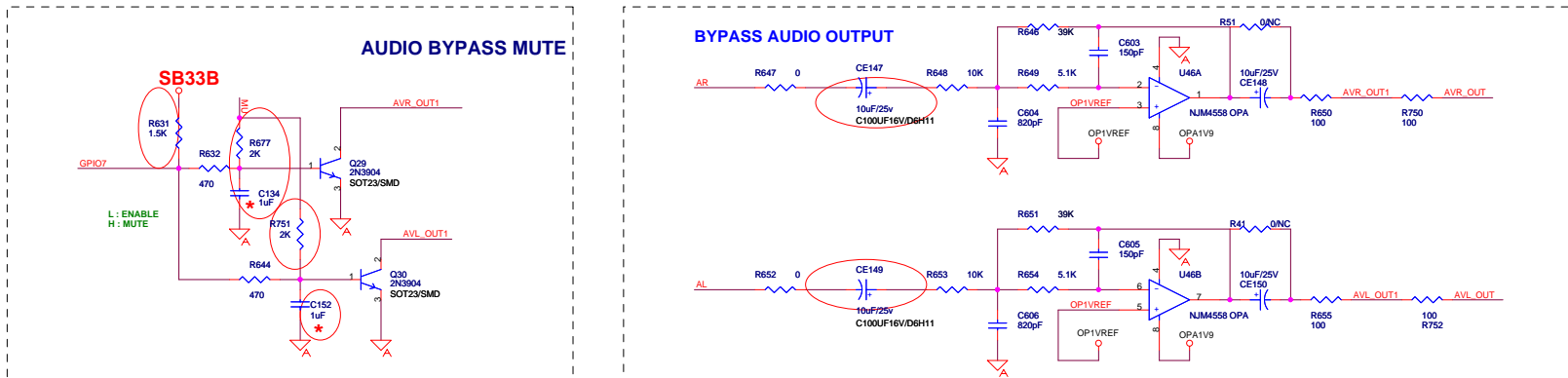
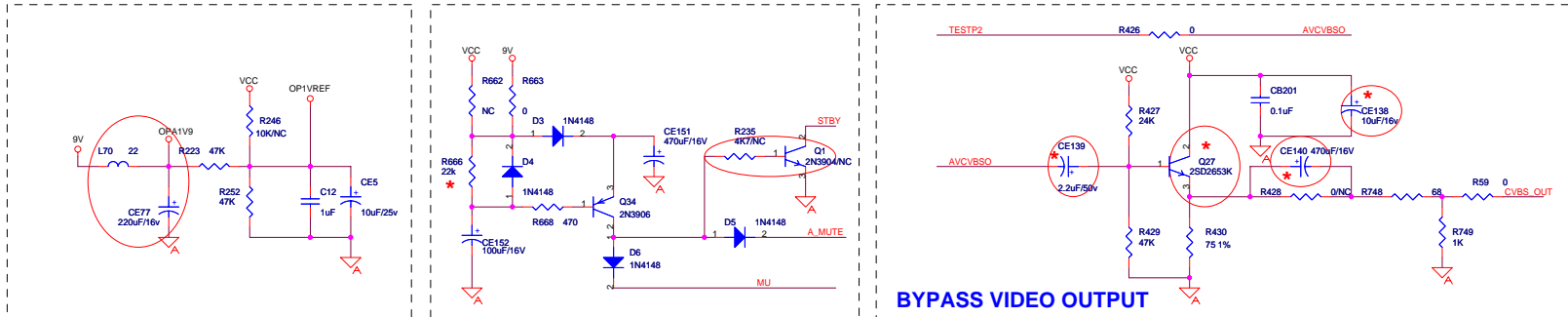
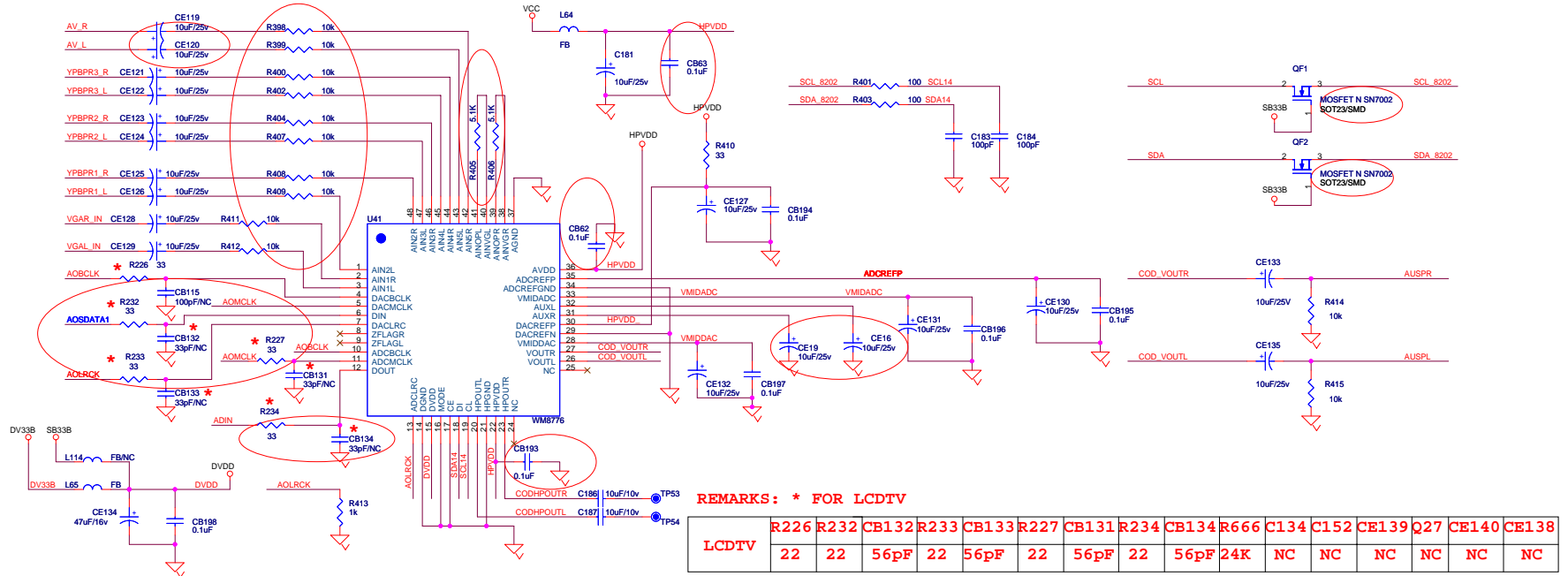
Title			
DAUGHTER BOARD IN			
Size	Document Number	<Designer>	Rev
C	AKAI_MT8202_27US_LVDS_V0.0	Checked: <Checker>	1
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INPUT

GPIO7	GPIO7	3
SCL	SCL	1,14
SDA	SDA	1,14
SDA_8202	SDA_8202	3,6,12
SCL_8202	SCL_8202	3,6,12
AOSDATA1	AOSDATA1	3
AOMCLK	AOMCLK	3,16
AOLRCK	AOLRCK	3,16
ADIN	ADIN	3,16
AV_L	AV_L	3
AV_R	AV_R	8
YPBPR1_L	YPBPR1_L	8
YPBPR1_R	YPBPR1_R	15
YPBPR2_L	YPBPR2_L	15
YPBPR2_R	YPBPR2_R	15
YPBPR3_L	YPBPR3_L	15
YPBPR3_R	YPBPR3_R	15
VGAR_IN	VGAR_IN	11
VGAR_OUT	VGAR_OUT	11
TESTP2	TESTP2	3
AR	AR	3
MU	MU	16
A.MUTE	A.MUTE	17
9V	9V	1,7,14

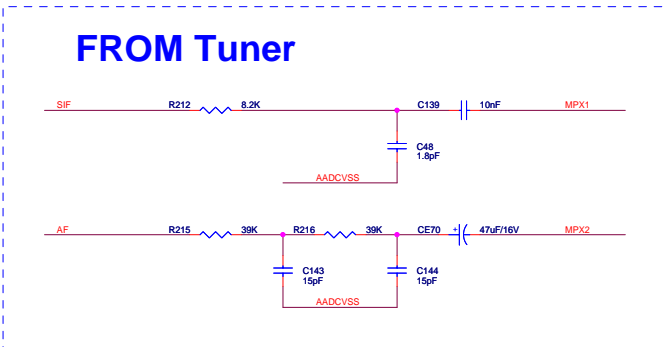
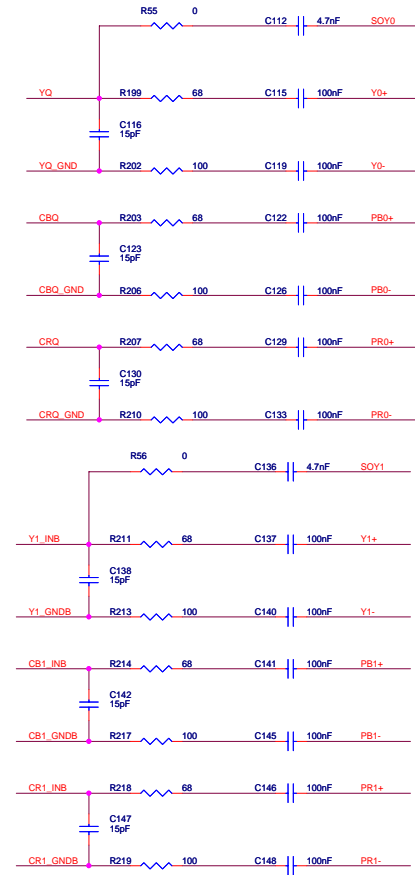
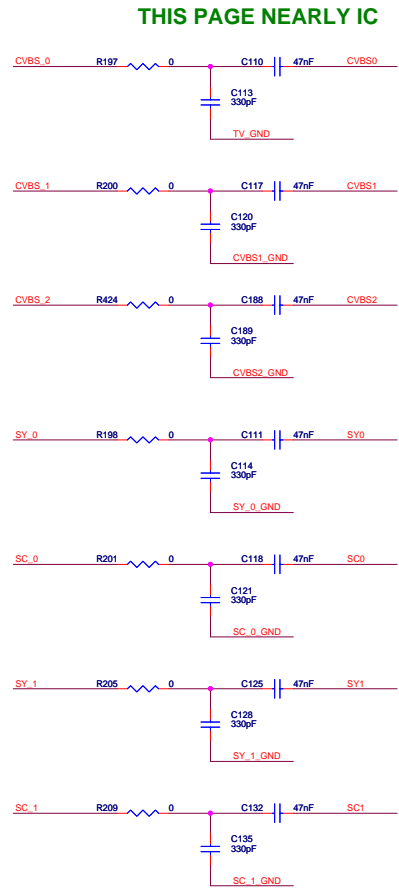
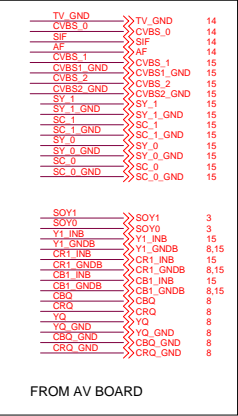
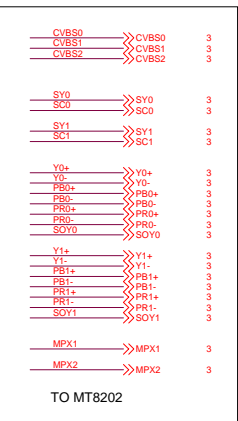
OUTPUT

AUSPR	AUSPR	16
AUSPL	AUSPL	16
AVR_OUT	AVR_OUT	15
AVL_OUT	AVL_OUT	15
CVBS_OUT	CVBS_OUT	6,15



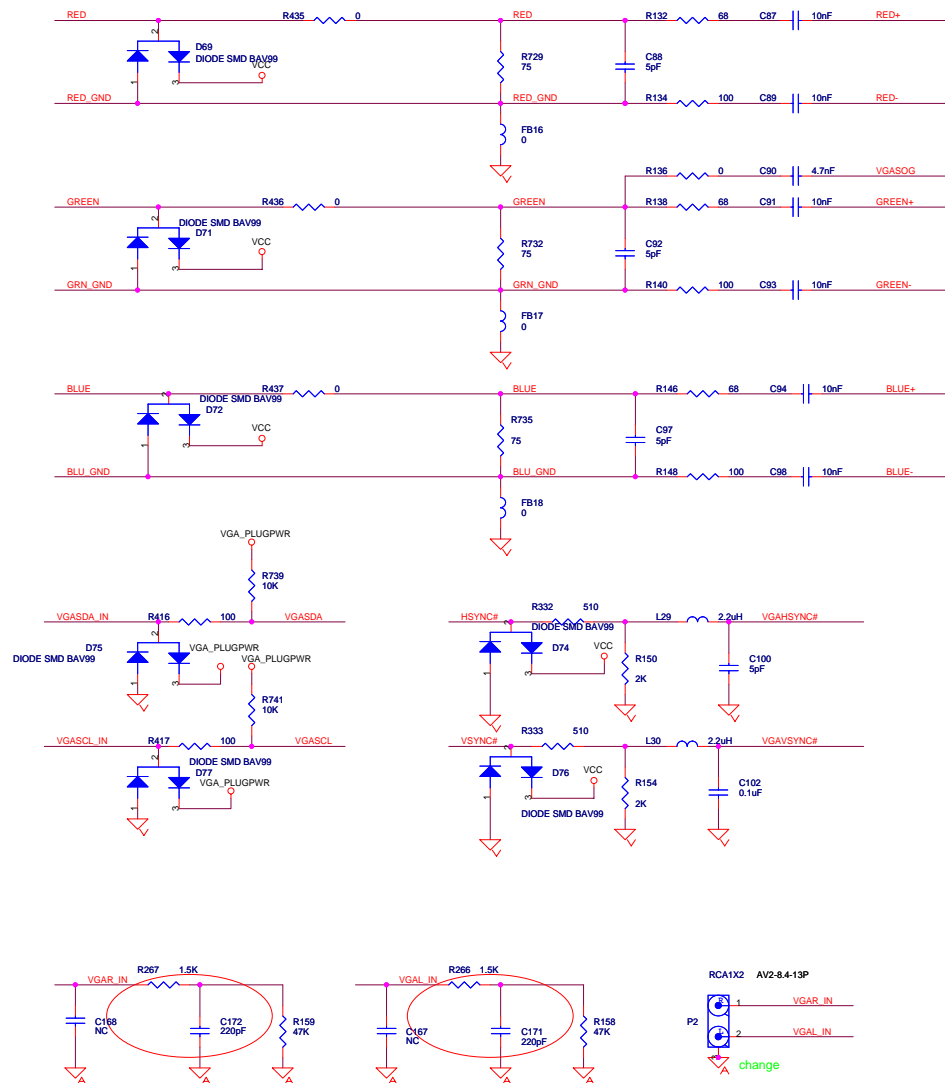
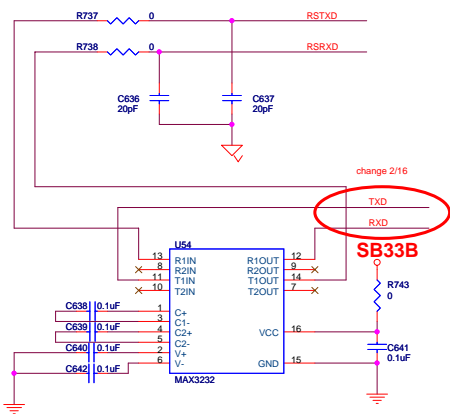
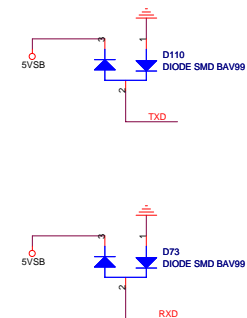
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File			
M8776 & VIDEO BYPASS			
Size	Document Number	AKAI_MT8202_27US_LVDS_V0.0	Rev 1
C	Checked:	Designer	Sheet 9
Date:	Saturday, April 22, 2006	Checked:	17



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File			
AUDIO / VIDEO IN CIRCUIT			
Size	Document Number	<Designer>	Rev
C	AKAI_MT8202_27US_LVDS_V0.0	Checked: <Checker>	1
Date:	Thursday, April 13, 2006	Sheet	17



RCA1X2 AV2-8.4-13P

P2

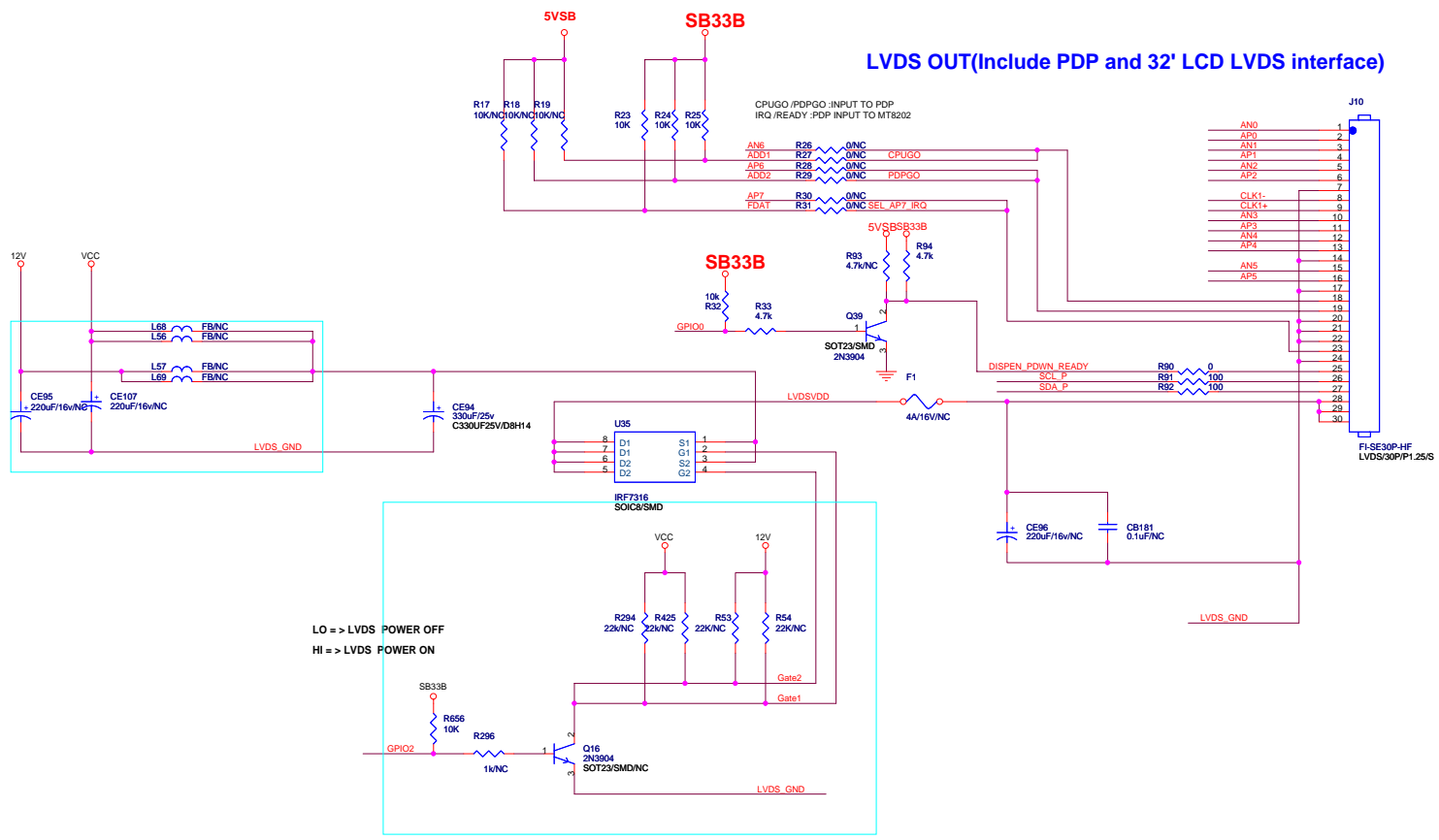
1 VGAR_IN

2 VGAL_IN

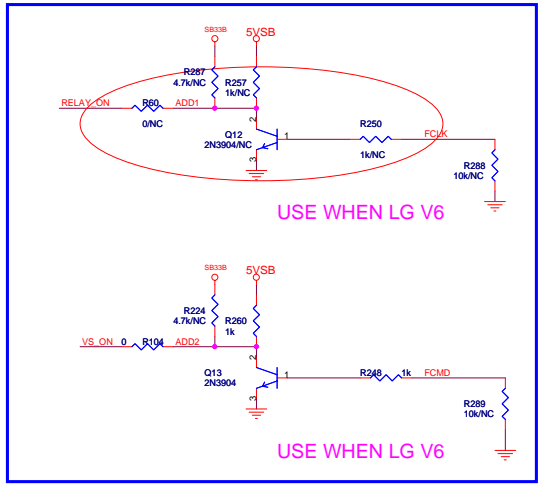
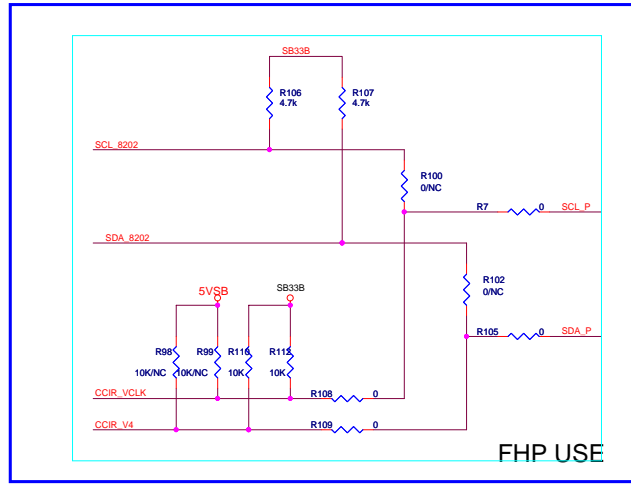
change

Title			
VGA IN & PC AUDIO IN			
Size	Document Number	Designer	Rev
C	AKAI_MT8202_27US_LVDS_V0.0	Checked: <Checker>	1
Date:	Thursday, April 13, 2006	Sheet 11	17

GPI00	>> GPI00	3
GPI02	>> GPI02	1,3
CLK1+	>> CLK1+	3
CLK1-	>> CLK1-	3
AP0_7	>> AP0_7	3
AP0_6	>> AP0_6	3
LVDS_GND	>> LVDS_GND	2,3,4
LVDS100	>> LVDS100	2,3,4
CCIR_VCLK	>> CCIR_VCLK	3
CCIR_V4	>> CCIR_V4	3
FCLK	>> FCLK	3
FCMD	>> FCMD	3
FDAT	>> FDAT	3
SCL_8202	>> SCL_8202	3,6,9
SDA_8202	>> SDA_8202	3,6,9
RELAY_ON	>> RELAY_ON	1
VS_ON	>> VS_ON	1
12V	>> 12V	1,13



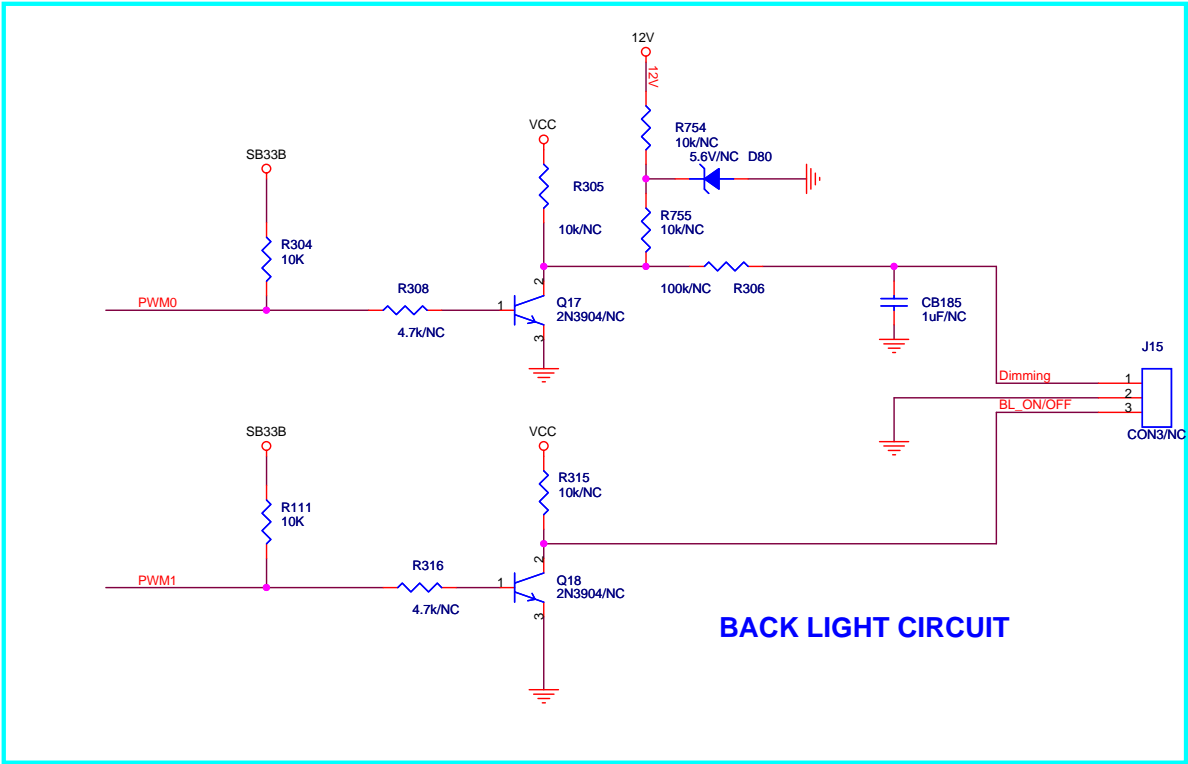
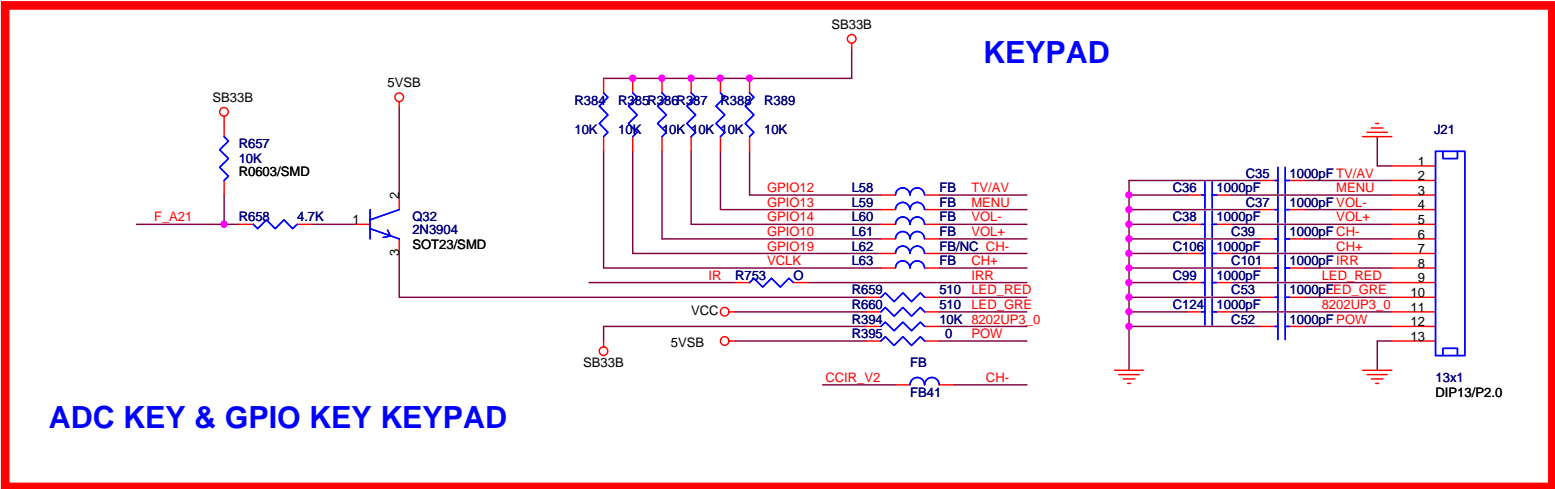
LO => LVDS POWER OFF
HI => LVDS POWER ON



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File			
LVDS OUT			
Size	Document Number	<Designer>	Rev
C	AKAI_MT8202_27US_LVDS_V0.0		1
Date:	Thursday, April 13, 2006	Checked: <Checker>	Sheet
		12	17

IR	>>>IR	3,15
GPIO10	>>>GPIO10	3
GPIO12	>>>GPIO12	3
GPIO13	>>>GPIO13	3
GPIO14	>>>GPIO14	1,3
PWM0	>>>PWM0	3
PWM1	>>>PWM1	3
8202UP3_0	>>>8202UP3_0	3
GPIO14	>>>GPIO14	1,3
GPIO19	>>>GPIO19	1,3
VCLK	>>>VCLK	3
F_A21	>>>F_A21	3
CCIR_V2	>>>CCIR_V2	3
12V	>>>12V	1,12

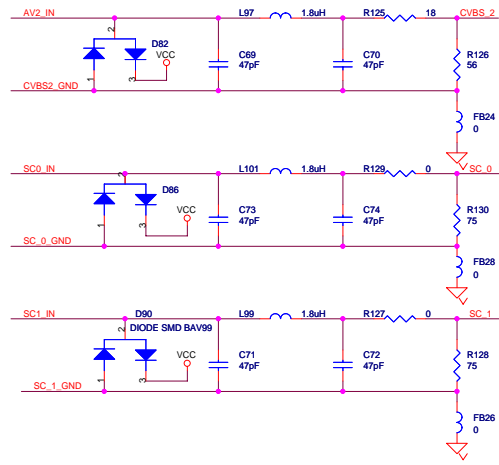
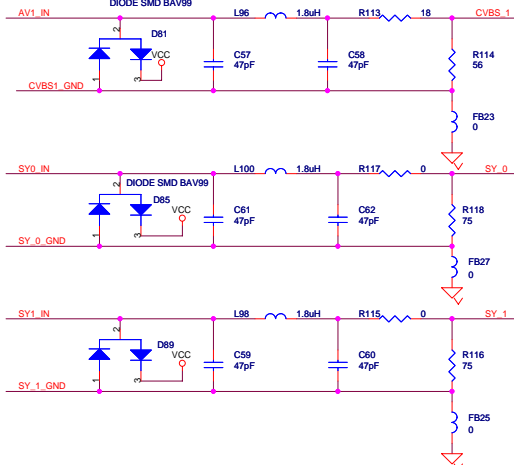
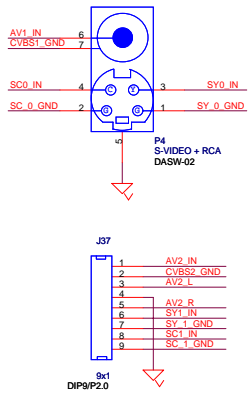


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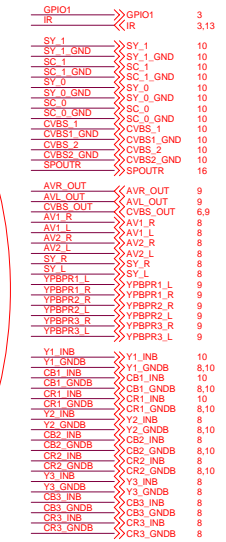
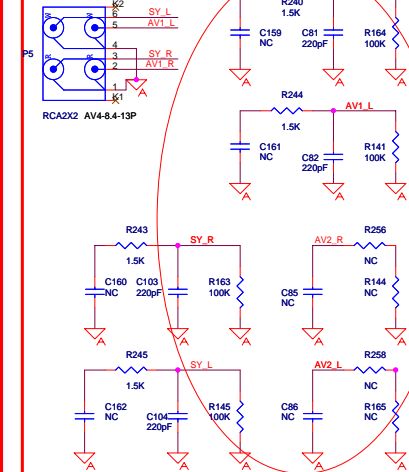
Title			
BACK LIGHT / KEYPAD			
Size B	Document Number	<Designer>	Rev
	AKAI_MT8202_27US_LVDS_V0.0	Checked: <Checker>	1
Date:	Thursday, April 13, 2006	Sheet	13 17



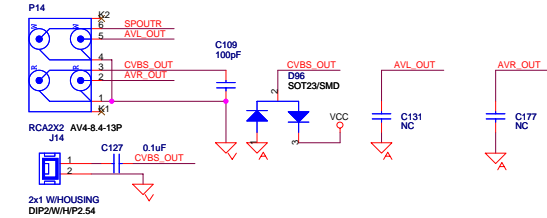
AV /YC VIDEO IN



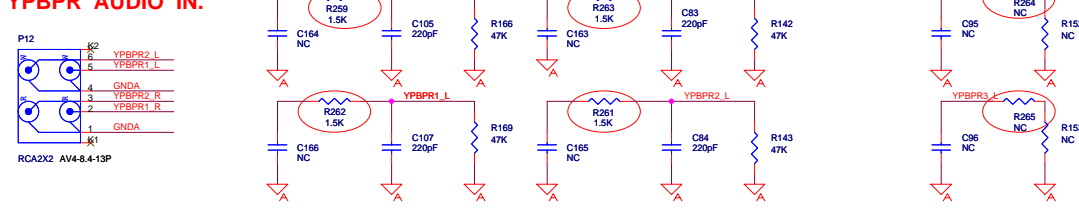
AV /YC AUDIO IN



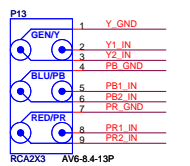
AV VIDEO/AUDIO OUT.



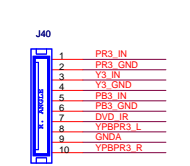
YPBPR AUDIO IN.



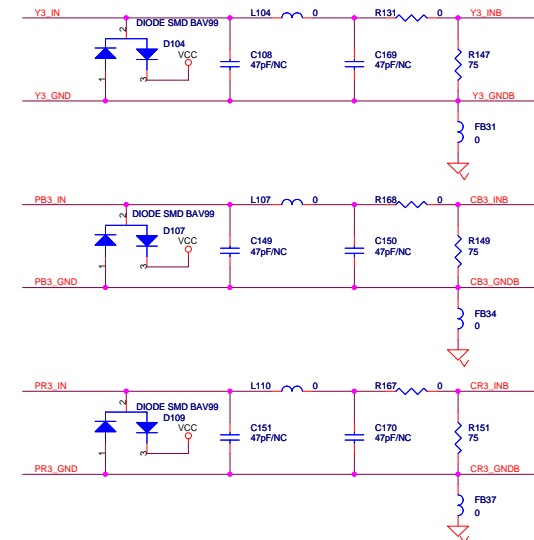
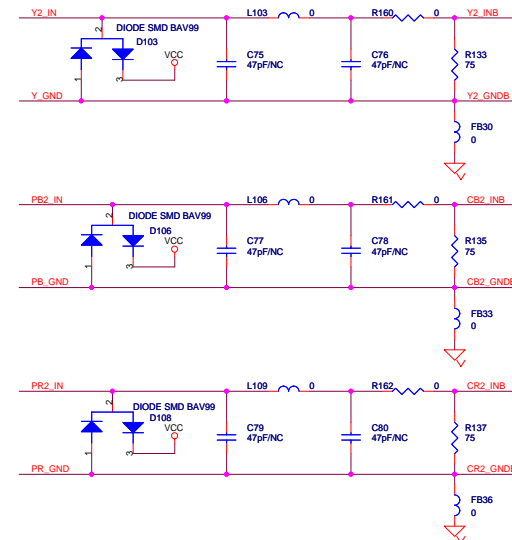
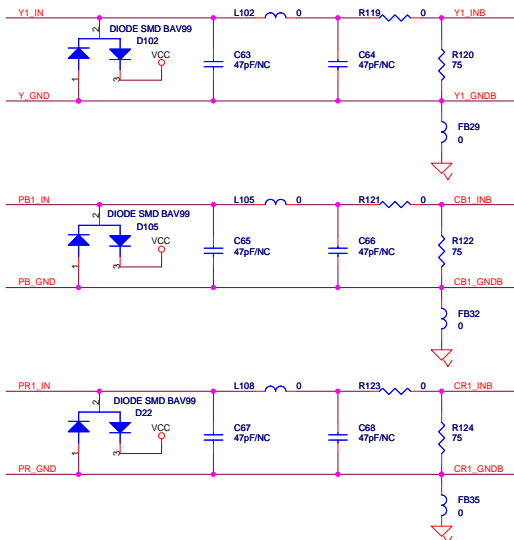
YPBPR VIDEO IN.



YPBPR1 / 2 INPUT.



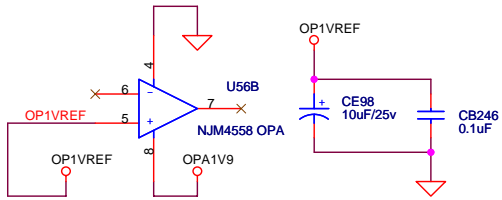
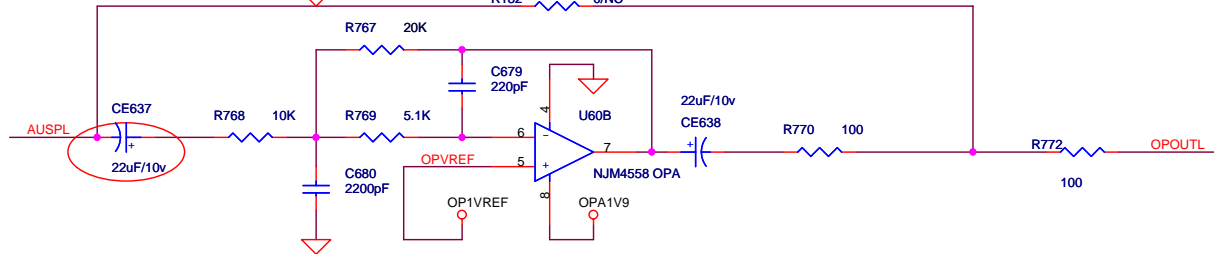
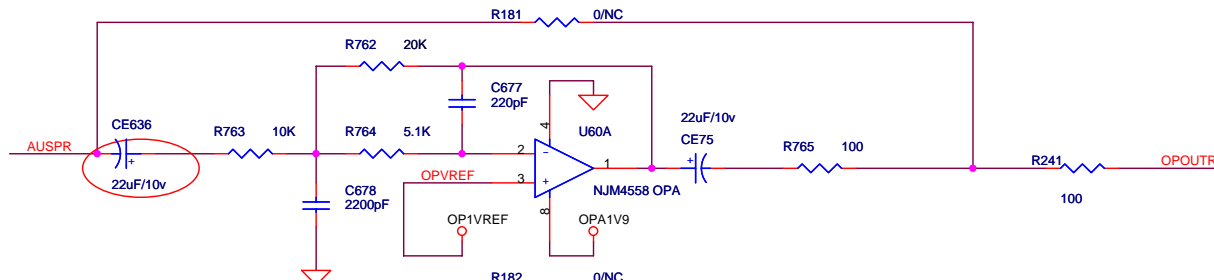
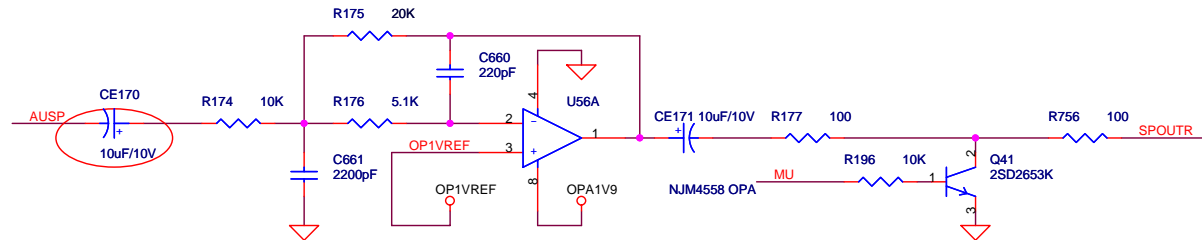
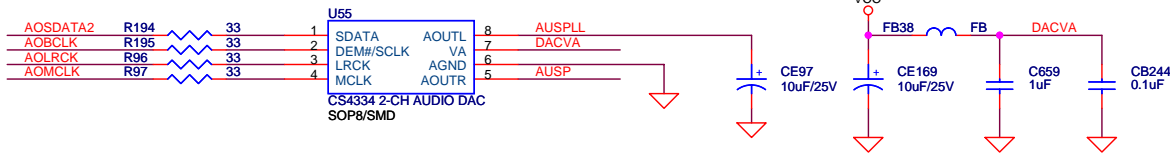
YPBPR 3 INPUT.



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File	AV IN	Designer	Rev
Size	Document Number	AKAI_M18202_27US_LVDS_V0.0	1
Date	Thursday, April 13, 2006	Checked: <Checker>	Sheet 15 of 17

AOSDATA2 >> AOSDATA2 3
 AOMCLK >> AOMCLK 3,9
 AOBCLK >> AOBCLK 3,9
 AOLRCK >> AOLRCK 3,9
 MU >> MU 9
 SPOUTR >> SPOUTR 15
 AUSPR >> AUSPR 9
 AUSPL >> AUSPL 9
 OPOUTR >> OPOUTR 17
 OPOUTL >> OPOUTL 17
 A_MUTE >> A_MUTE 9,17



GPIO DECIPTION

UP3_4 : SW SCL
 UP3_5 : SW SDA
 ERO0/UP3_0 :KEYPAD POWER
 ERO1/UP3_1 : MAIN POWER SWITCH
 VCLK : KEPAD CH+
 GPIO19 : KEPAD CH-
 DE/GPIO : DVD IR
 CCIR_CLK : PDP USE
 CCIR_V4 : PDP USE
 GPIO0 : PDP USE
 GPIO1 : NO USE
 GPIO2 : LVDS POWER SW
 GPIO3 : DTV POWER CONTROL
 GPIO4 : EEPROM WRITE PROTECT
 GPIO5/TXD : 2nd UART FOR MT5351
 GPIO6/RXD : 2nd UART FOR MT5351
 GPIO7 : AUDIO BYPASS MUTE CONTROL
 GPIO8 : SPEAKER SWITCH
 GPIO9 : AUDIO MUTE
 GPIO10 : Indicates active video at HDMI port
 GPIO11 : DVD POWER CONTROL
 GPIO12 : AV SWITCH
 GPIO13 : HDMI Hot Plug Detect
GPIO14 : NO USE
 GPIO[15..18] : FOR DVD CONTROL
 GPIO/PWM0 : DIMMING
 GPIO/PWM1 : BACKLIGHT ON/OFF
 OUT_27Mhz/GPIO : HDMI CRYSTAL
 SDA1 : TO MT5351 I/F REQUEST
 SCL1 : TO MT5351 I/F READY
 F_A21 : KEYPAD(LED RED)
 ADCIN0 : KEYPAD
 ADCIN3:PDP 5VD DETECT
 ADCIN4:FOR TUNER AFC
 CCIR_V[0-3] : KEYPAD
 CCIR_V5 : AUDIO SWITCH
 CCIR_V6 : RESET DTV
 CCIR_V7 : YBPBR VIDEO SWITCH

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Title			
SUB WOOFER			
Size	Document Number	<Designer>	Rev
B	AKAI_MT8202_27US_LVDS_V0.0	Checked: <Checker>	1
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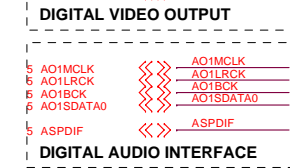
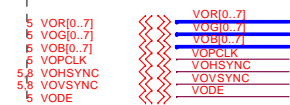
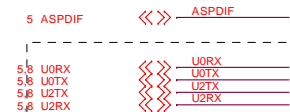
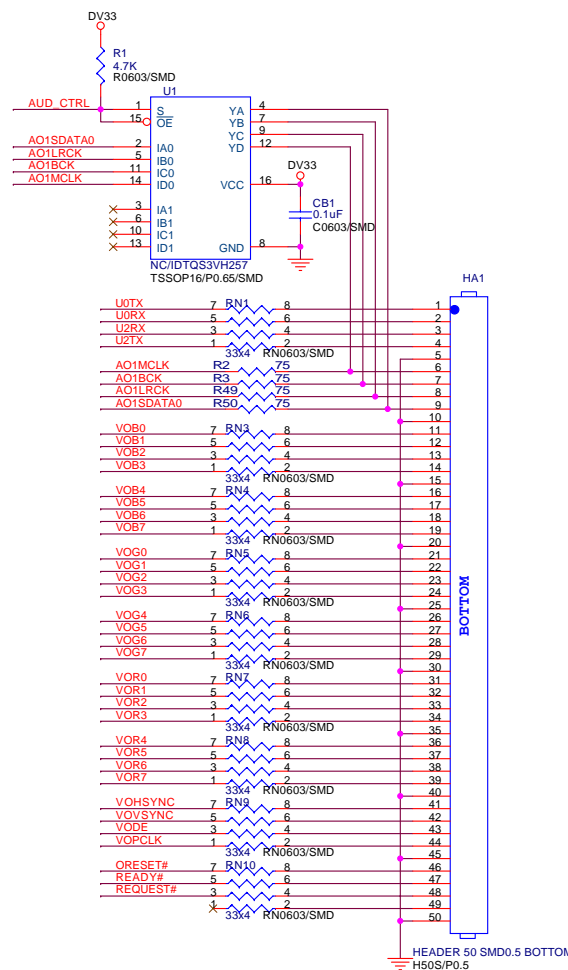
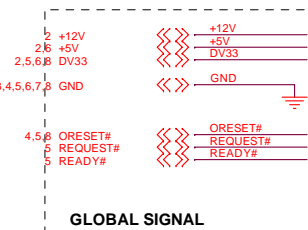
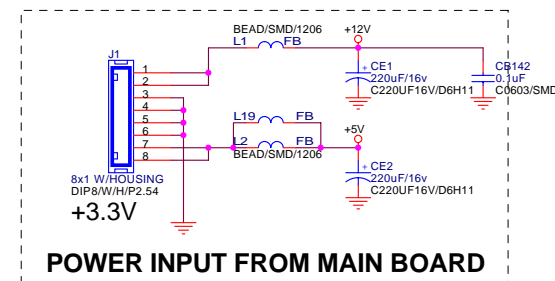
MT5111 / MT5351 REFERENCE DESIGN - 4 LAYERS

Rev	History	P#	DATE
RA-V1	INITIAL VERSION		2005/06/15
RA-V2	ADDED AUDIO SWITCH / REFINE POWER CIRCUIT		2005/07/14

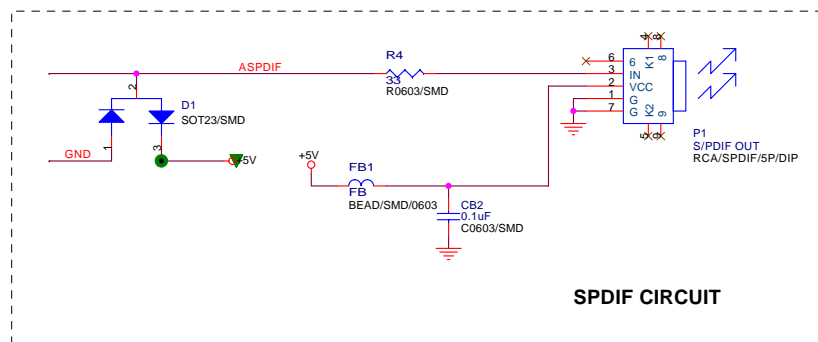
01. INDEX AND INTERFACE
02. POWER
03. TUNER
04. MT5111 ASIC
05. MT5351 ASIC
06. MT5351 PERIPHERAL
07. DDR MEMORY
08. NOR FLASH / JTAG / UART

NS : NON-STUFF

NAME	TYPE	DEVICE
+12V	POWER +12V	POWER SUPPLY
+5V	POWER +5V	POWER SUPPLY
+5V_tuner	POWER +5V	TUNER POWER
DV33_DM	POWER +3V3	MT5111 POWER
DV18	POWER +1V8	MT5111 POWER
DV33	POWER +3V3	MT5351 POWER
AV33	POWER +3V3	MT5351 ANALOG POWER
DV25	POWER +2V5	MT5351 DDR POWER
DV12	POWER +1V2	MT5351 POWER
GND	GROUND	GROUND

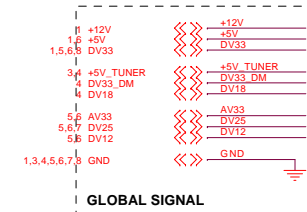
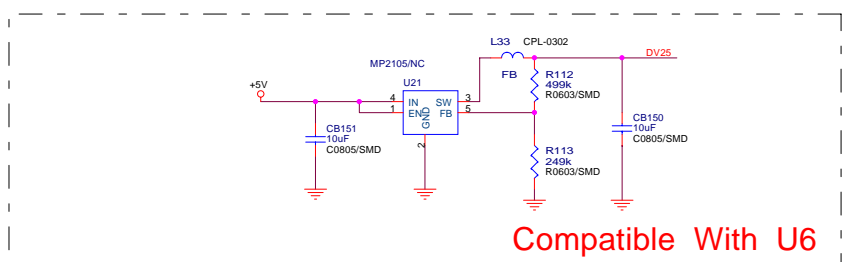
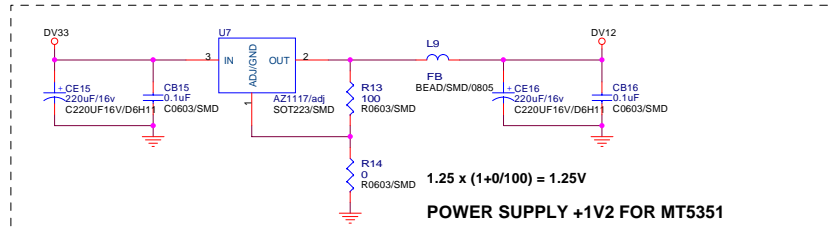
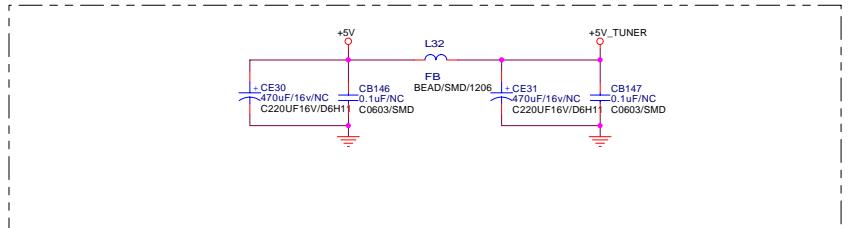
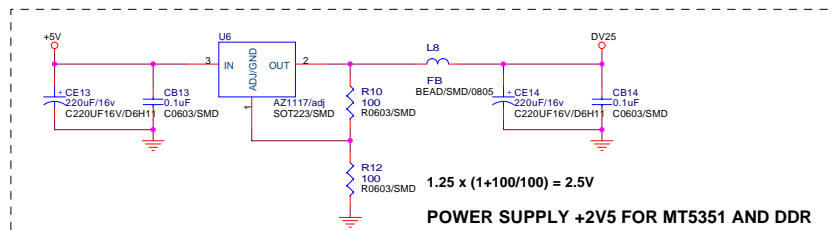
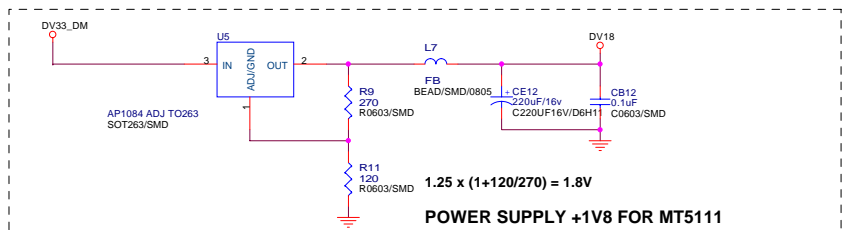
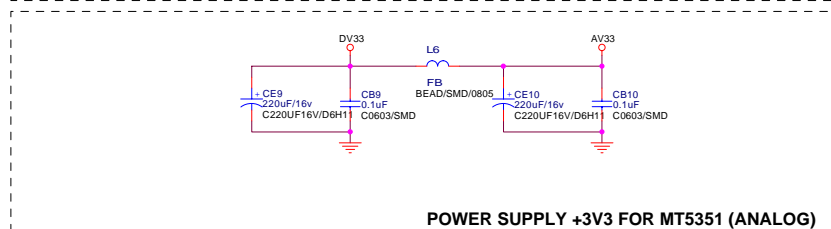
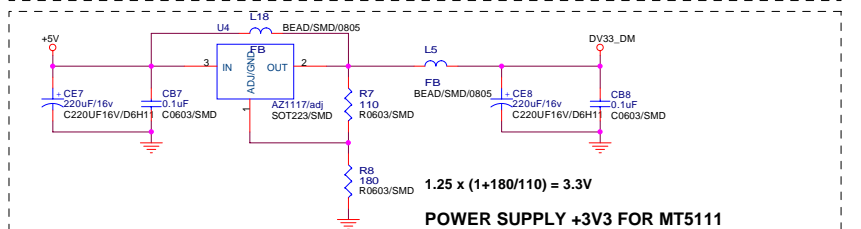
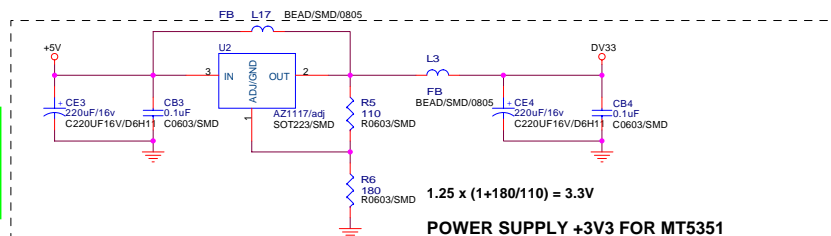
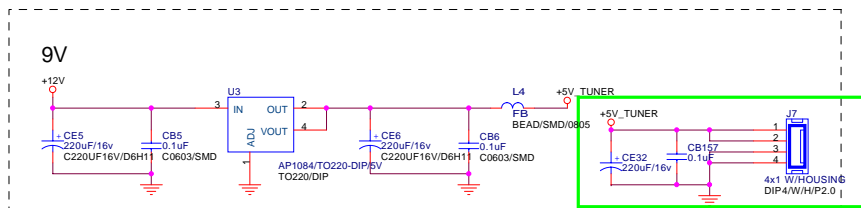


DIGITAL OUTPUT



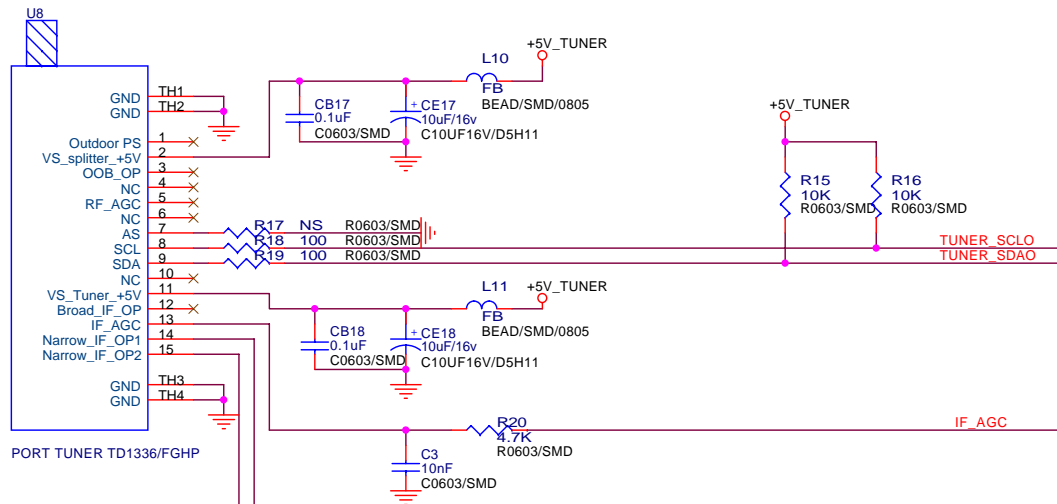
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Title INDEX			
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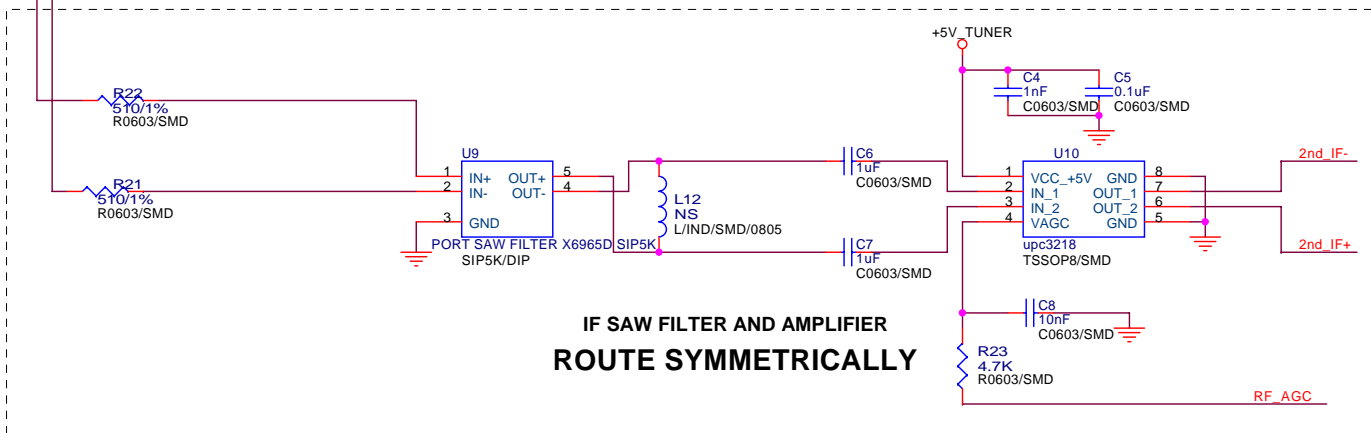


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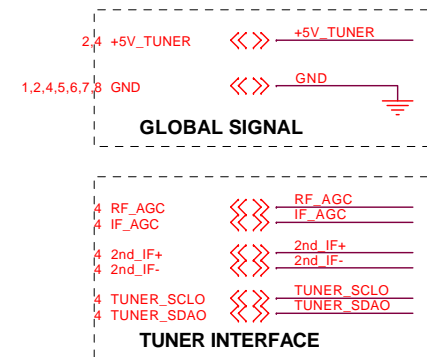
POWER				
Size	Document Number	MT5351RA-V2		Rev
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PORT TUNER TD1336/FGHP

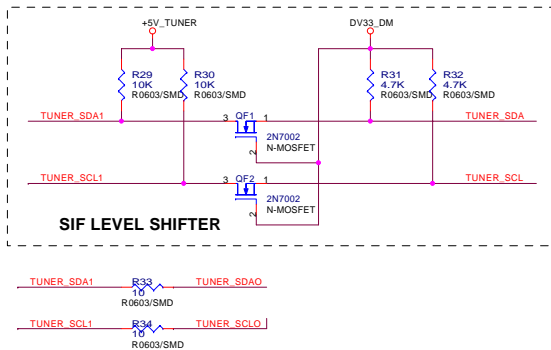
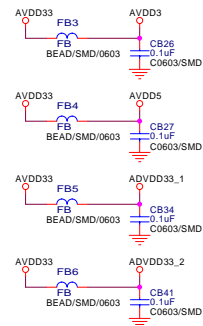
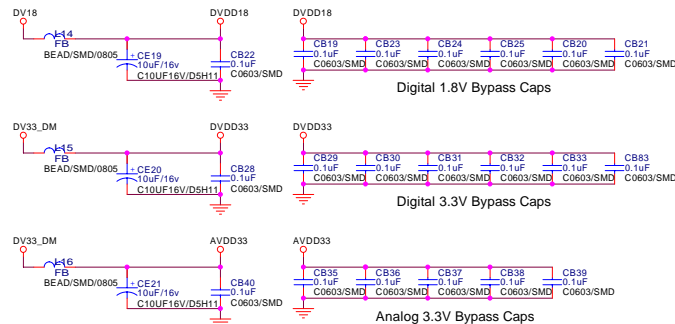
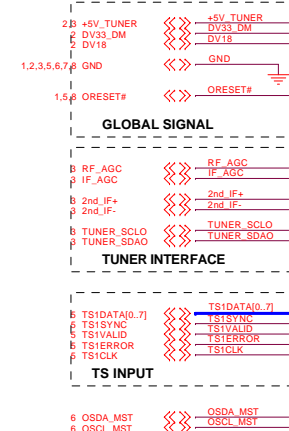
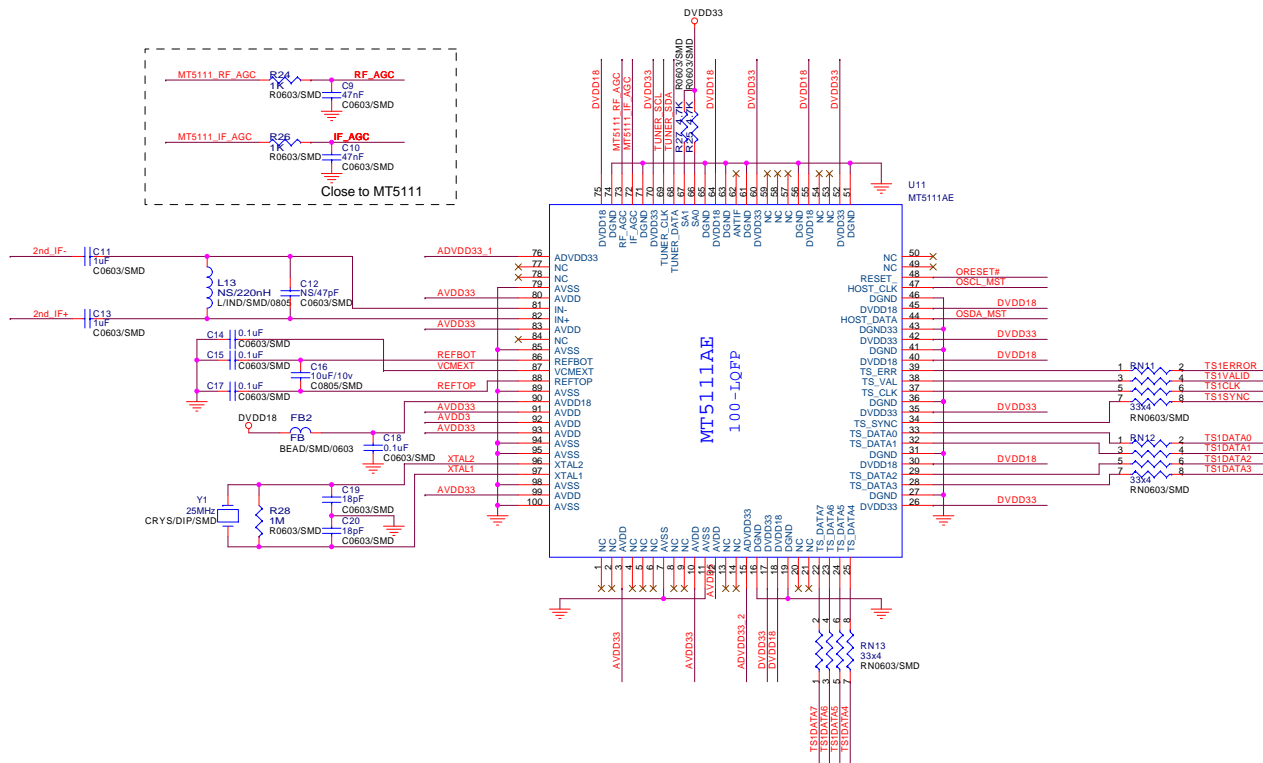


IF SAW FILTER AND AMPLIFIER
ROUTE SYMMETRICALLY



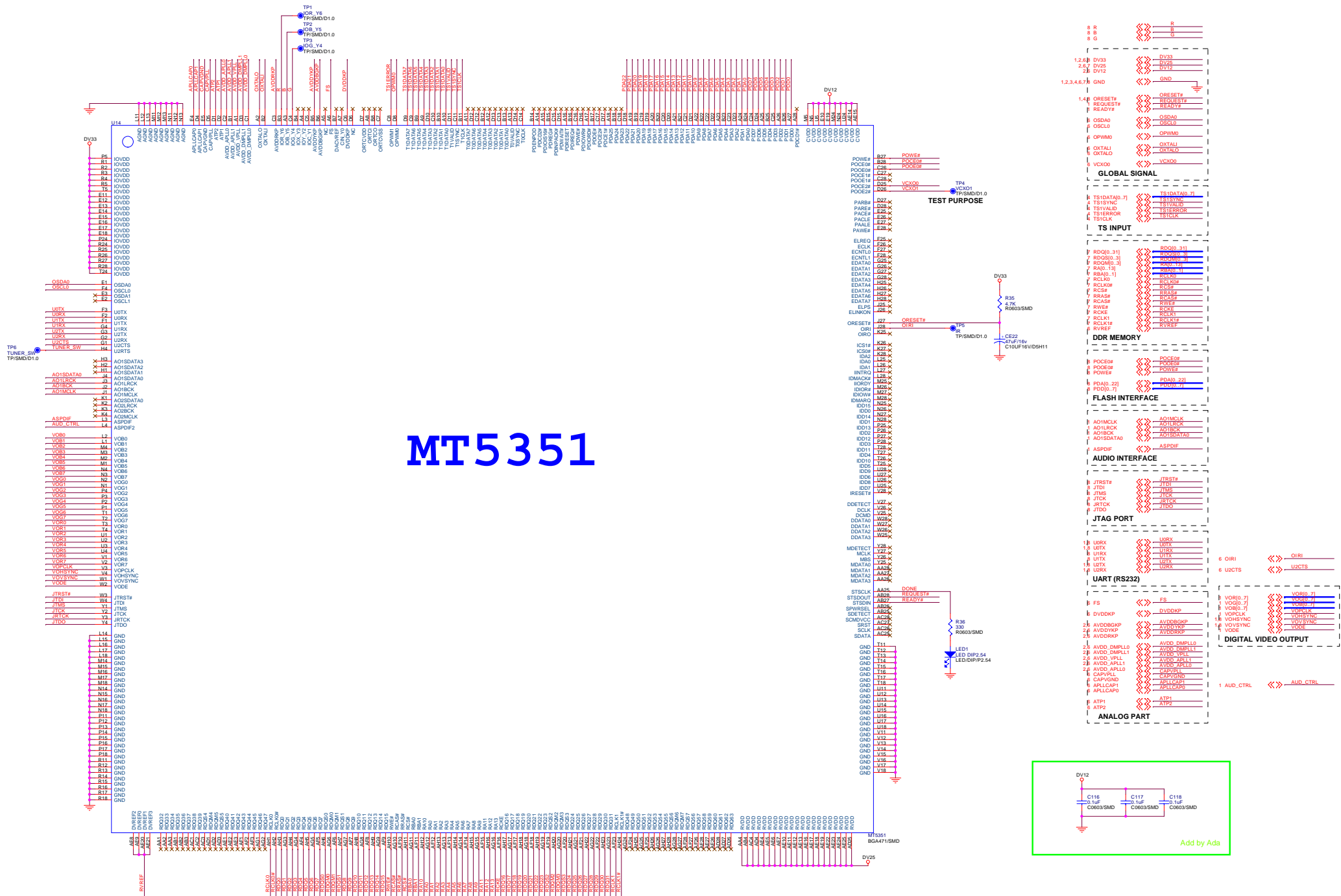
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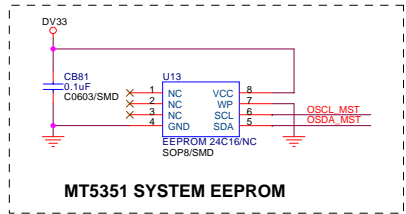
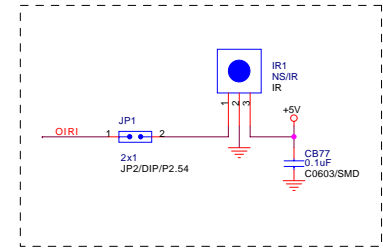
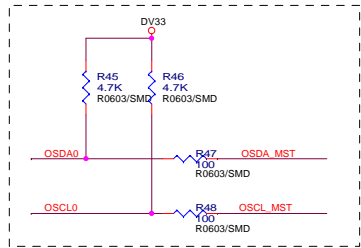
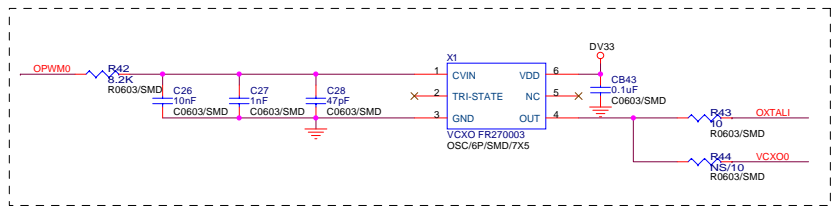
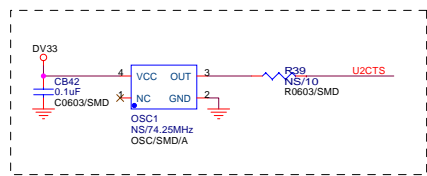
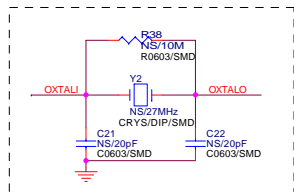
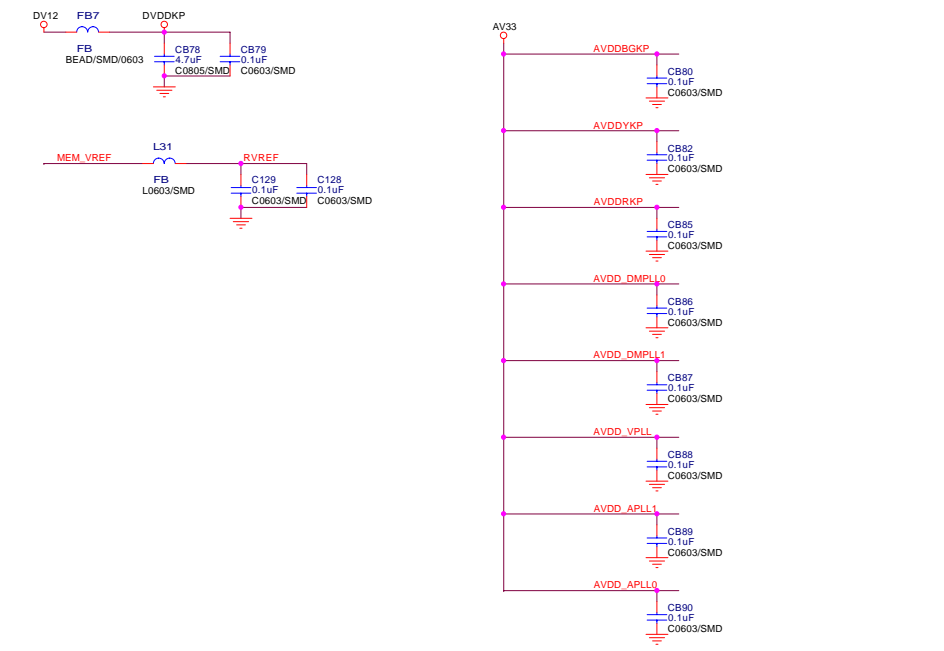
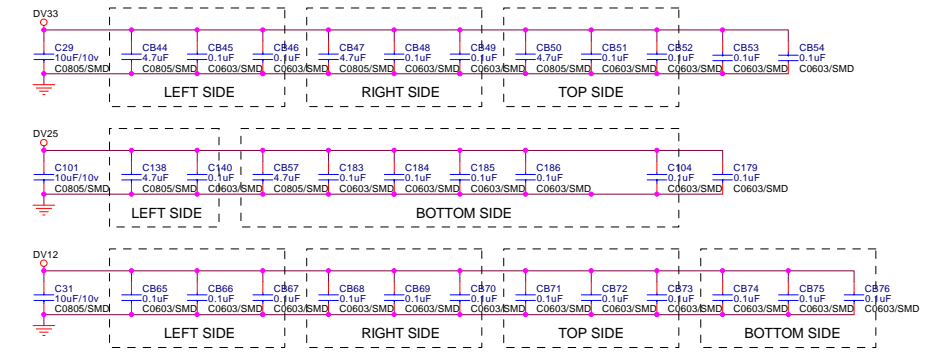
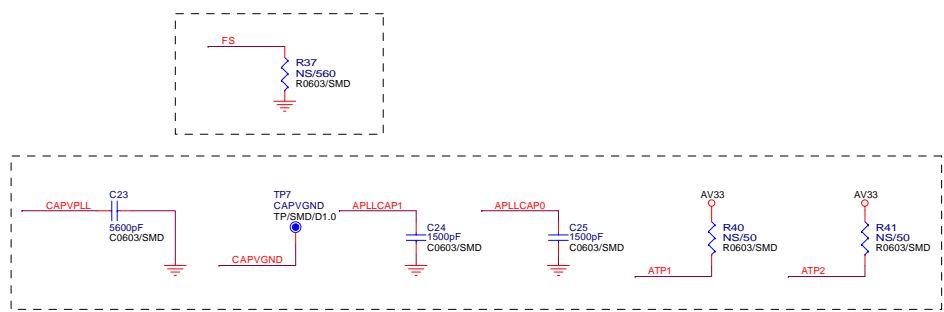
Title			
TUNER			
Size	Document Number	Rev	
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File			
MT5111 ASIC			
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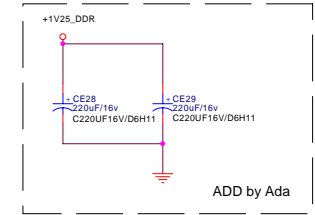
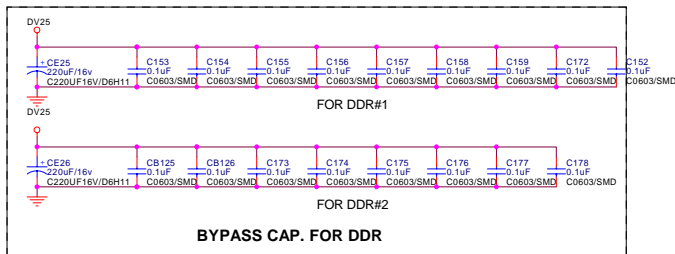
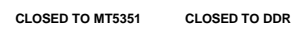
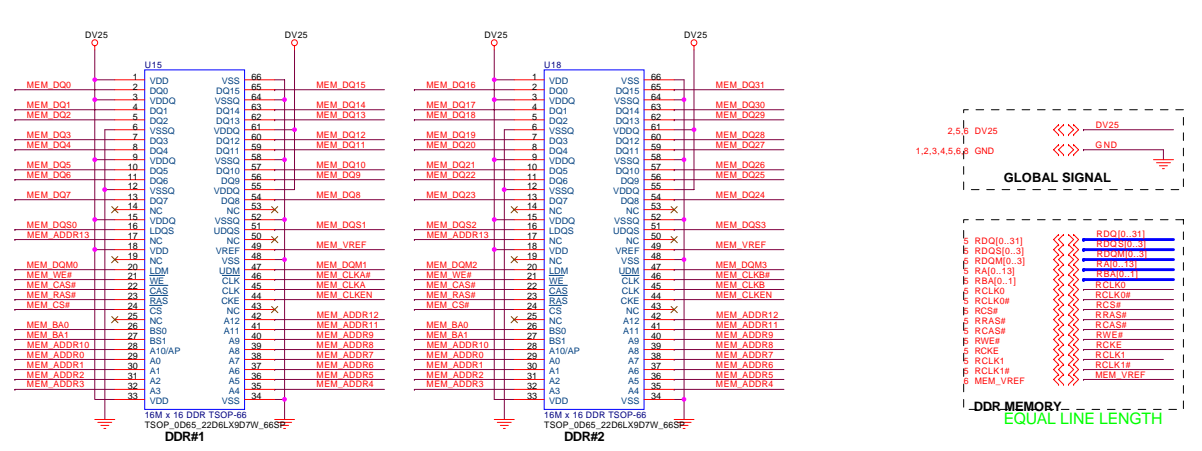




1P	+5V	<<>>	+5V
1,2,5,8	DV33	<<>>	DV33
2,6	AV33	<<>>	AV33
2,5,7	DV25	<<>>	DV25
2,5	DV12	<<>>	DV12
1,2,3,4,5,7,8	GND	<<>>	GND
6	OSDA0	<<>>	OSDA0
6	OSCL0	<<>>	OSCL0
4	OSDA_MST	<<>>	OSDA_MST
4	OSCL_MST	<<>>	OSCL_MST
GLOBAL SIGNAL			
6	FS	<<>>	FS
5	DVDDKP	<<>>	DVDDKP
2,6	AVDDBGKP	<<>>	AVDDBGKP
2,6	AVDDYKP	<<>>	AVDDYKP
2,6	AVDDRKP	<<>>	AVDDRKP
1	AVDD_DMPLLO	<<>>	AVDD_DMPLLO
2,6	AVDD_DMPLLI	<<>>	AVDD_DMPLLI
2,6	AVDD_VPLL	<<>>	AVDD_VPLL
2,6	AVDD_APLL1	<<>>	AVDD_APLL1
2,5	AVDD_APLL0	<<>>	AVDD_APLL0
6	CAPVPLL	<<>>	CAPVPLL
6	CAPVGNND	<<>>	CAPVGNND
6	APLLCAP1	<<>>	APLLCAP1
6	APLLCAP0	<<>>	APLLCAP0
6	ATP1	<<>>	ATP1
6	ATP2	<<>>	ATP2
ANALOG PART			
7	MEM_VREF	<<>>	MEM_VREF
5	RVREF	<<>>	RVREF
5	OPWM0	<<>>	OPWM0
5	OXTALI	<<>>	OXTALI
5	OXTALO	<<>>	OXTALO
5	VCX00	<<>>	VCX00
5	U2CTS	<<>>	U2CTS
5	OIRI	<<>>	OIRI

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Title			
MT5351 PERIPHERAL			
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Basic Operations & Circuit Description

MODULE

There are 1 pcs panel and 5 pcs PCB including 3 pcs Extension PCB, 1 pcs Timming controller board and 1 pcs Back Light board in the Module.

SET

There are 6 pcs PCBs including 1 pcs ATV Tuner board, 1 pcs keypad board, 1 pcs Remote Control Receiver board, 2 pcs L/R Speakers and 1 pcs Main(Video)board, 1 pcs ATSC board in the SET.

PCB funtion

1. Power :

(1). Input voltage: AC 120V, 60Hz.

(2). To provide power for PCBs.

2. Main board : To converter TV signals, S signals, AV signals, Y Pb/Cb Pr/Cr signals, DVI/HDMI signals and D-SUB signals to digital ones and to transmit to Control board.

3. Control board : Dealing with the digital signal for output to panel.

4. Extension board : Output addressing signals.

5. ATV Tuner Board : To convert TV RF signal to video and SIF audio signal to Main board.

6. ATSC Board : Receiver and converter ATSC TV signal to transmit to main board.

PCB failure analysis

1. CONTROL : a. Abnormal noise on screen. b. No picture.
2. MAIN :
 - a. Lacking color, Bad color scale.
 - b. No voice. (Make sure status: Mute / Internal, External speaker)
 - c. No picture but with signals output, OSD and back light.
 - d. Abnormal noise on screen.
3. POWER : NO picture, no power output.
4. Back Light :
 - a. No picture.
 - b. Flash on screen.
 - c. Darker picture with signals.
5. ATV Tuner :
 - a. No ATV Noise
 - b. No ATV signals
6. ATSC: a No ATSC TV signal

Main IC Specifications

- M13S128168A (ESMT)
2M x 16 Bit x 4 Banks Double Data Rate SDRAM
- MT5111CE
Single-Chip HDTV/CATV Demodulator
- MT5351
MT5351 is a DTV Backend Decoder SOC which support flexible transport demux, HD MPEG-2 video decoder, MPEG1,2, MP3, AC3 audio decoder, HDTV encoder. MT5351 is powered by ARM 926EJ with 16K I-Cache and 16K D-Cache. It can support 64Mb to 1Gb DDR DRAM devices with configurable 32/64 bit data bus interface.
- MT8202
MT8202G is a highly integrated Single-Chip for LCD TV supporting video input and output format up to HDTV. It includes 3D comb filter TV decoder to retrieve the best image from popular composite signals.
- MT8293
HDMI PanelLink Cinema Receiver
- R2S15102NP
Digital Power Amplifier R2S15102NP
- WM8776
24-bit, 192kHz Stereo CODEC with 5 Channel I/P Multiplexer

MT5111CE

Single-Chip HDTV/CATV Demodulator

Key Features

- Compliant with ATSC digital television standard
- Supports SCTE DVS-031 and ITU J.83 Annex B digital CATV standard
- Accepts direct IF (44 MHz or 43.75MHz) and low IF (5.38MHz)
- Differential IF input with programmable input signal level: 0.5Vpp to 2Vpp
- NTSC interference rejection capability
- Compensate echo up to -5 to +47 μ s range for terrestrial HDTV reception
- On-chip 10-bit ADC for HDTV/CATV demodulator
- On-chip programmable gain amplifier
- 25MHz crystal for clock generation
- On-chip PLL clock generation
- Full-digital timing recovery, no VCXO is required
- Full-digital frequency offset recovery with wide acquisition range ± 1 MHz for ATSC and ± 250 KHz for CATV reception
- Dual digital AGC controls for IF and RF respectively
- MPEG-2 transport stream output in parallel or serial format
- On-chip error rate estimators for TS packets, TCM decoder, and equalizer
- EIA/CEA-909 antenna interface
- Controlled by I²C interface
- Supports sleep mode to save power consumption
- Core power supply: 1.8V, peripheral power supply: 3.3V
- 100-LQFP package
- Lead Free

Functional Block Diagram

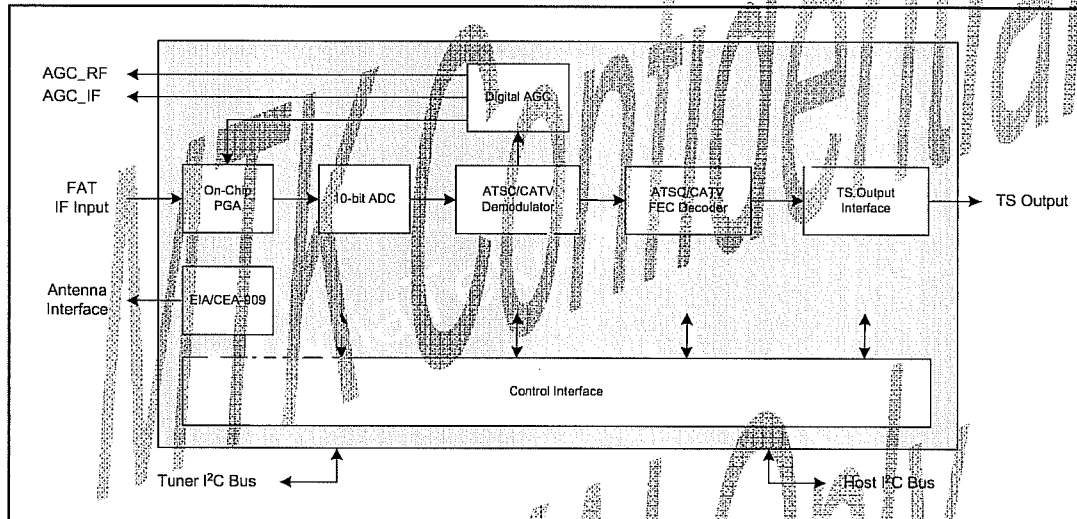


Figure 1: MT5111CE Functional Block Diagram

General Description

MT5111CE is a fully integrated single-chip 8-VSB and 64/256-QAM demodulator. The chip is designed specifically for the digital terrestrial HDTV and CATV receivers, and is fully compliant with ATSC A/53, SCTE DVS-031, and ITU J.83 Annex B standards.

MT5111CE includes a 10-bit A/D converter, 8-VSB/QAM demodulator, TCM (Trellis-Coded Modulation) decoder, and Reed-Solomon Forward Error Correction decoder. Moreover, an internal controller handles the acquisition and tracking to ensure the best receiving performance. The internal controller communicates with the external host controller via the I2C-compatible interface, and also provides direct control to the RF tuner via the second I2C-compatible

interface.

MT5111CE accepts either the direct IF signals centered at 44MHz or 43.75MHz, or the low IF signals centered at 5.38MHz. The center frequency of the incoming IF signal can also be programmed to other frequencies for various applications. An On-chip programmable gain-controlled amplifier is designed to provide sufficient signal amplitude when the received RF signal is weak. The IF signal is first sampled by a 10-bit A/D converter. Afterward, the digitized samples are further processed for adjacent channel interference rejection.

MT5111CE measures the power level of the digitized sequence, and feeds the control voltages back to the RF tuner and the IF amplifier respectively. The control voltages are converted to analog signals through the on-chip 1-bit sigma-delta D/A converters plus the off-chip R-C low-pass filters. The automatic gain control keeps the received power level at a desired level and maximizes the received SNR.

The carrier frequency offset and symbol timing offset are both estimated and compensated by a fully digital synchronizer. The synchronizer also controls the rate conversion in the digital re-sampling device by estimating the sampling frequency offset. All synchronization in MT5111CE are integrated in digital circuits, no external VCXO is required.

The equalizer is adopted to cancel the effect of multi-path fading channel during signal propagation in the air or over cable networks. The equalizer is not only capable of acquiring correct coefficients combination by specified adaptive algorithms, but also programmable to different configurations for various channel conditions.

The following FEC decoder corrects most of the errors by the concatenation

of TCM and Reed-Solomon decoders. For CATV reception, MT5111CE detects and aligns de-puncturing timing of the received sequence. The timing synchronization is also automatically performed to lock the FEC frames. The on-chip error rate estimator can simultaneously monitor the receiving qualities at the three stages: equalizer output, TCM decoder, and transport stream packets. The chip finally outputs the decoded MPEG-2 packets in either the serial or parallel transport stream format.

In addition to the demodulation of HDTV signal, MT5111CE also provides the capability to remove the NTSC co-channel interference. To achieve the best reception condition, an antenna interface compliant with EIA/CEA-909 is designed to control the antenna parameters.

MT5111CE is designed with efficient mechanisms of power saving. When configured to enter the sleep mode by the system host, it can immediately turn off almost all embedded hardware except the on-chip controller to reduce the power consumption. Resuming from sleep mode is also triggered by the system host. Upon returning to the operation mode, the chip will try to re-acquire the DTV signal automatically.

Pin Out

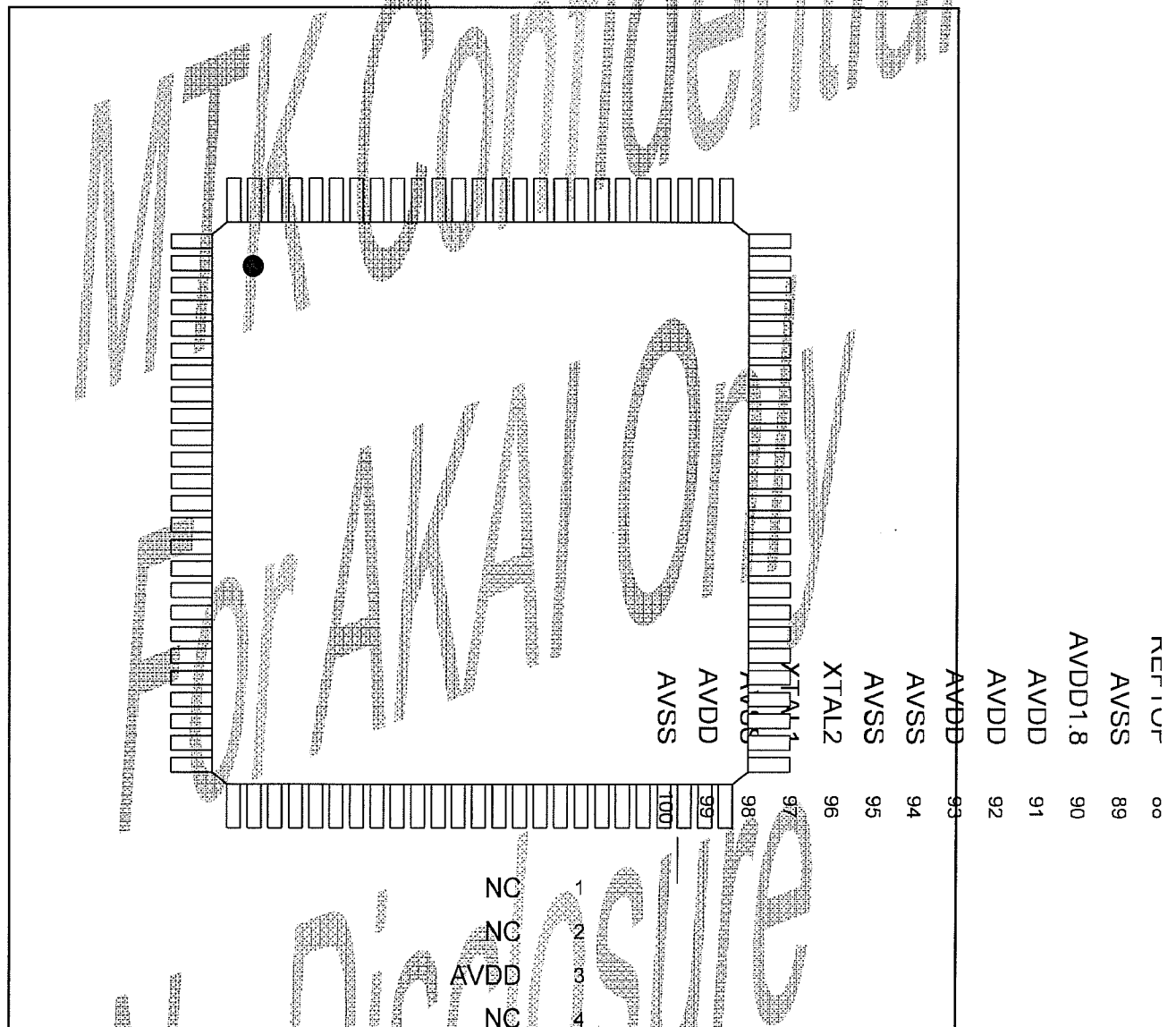


Figure 2: MT5111CE Pin Out

Pin Description

Signal Name	Pin No	I/O	Description
Transport Stream			
TSDATA[7:0]	22,23,24,25,28,29,32,33	O	TS data output
TSSYNC	34	O	TS packet start signal
TSVAL	38	O	TS output valid signal
TSCLK	37	O	TS output clock
TSERR	39	O	TS packet error indicator
Analog Signal			
IN+	82	I	Analog differential IF input
IN-	81	I	
REFTOP	88	O	ADC reference top voltage. Decouple with a capacitor to AVSS
REFBOT	86	O	ADC reference bottom voltage. Decouple with a capacitor to AVSS
VCNEXT	87	O	ADC common mode voltage
Antenna Interface			
ANTIF	62	O	CEA-909 Antenna Control Interface
Clock Generation			
XTAL1	97	I	25MHz crystal input
XTAL2	96	I	
Control Signals			
HOST_CLK	47	I	Host processor serial clock input, 5 volt compatible
HOST_DATA	44	I/O	Host processor serial data pin, 5 volt compatible
TUNER_CLK	69	O	Tuner serial clock output, 5 volt compatible
TUNER_DATA	68	I/O	Tuner serial data pin, 5 volt compatible
IF_AGC	72	O	IF AGC output
RF_AGC	73	O	RF AGC output
RESET	48	I	Power reset pin, low active
SA0	66	I	Chip slave address selection pin, tie to VDD3.3 or DGND
SA1	67	I	Chip slave address selection pin, tie to VDD3.3 or DGND
Power Supply			
VDD3.3	17,26,35,42,52,60,70	P	Digital power supply, tie to 3.3V
VDD1.8	18,30,40,45,55,64,75	P	Digital power supply, tie to 1.8V
DGND	16,19,27,31,36,41,43,46,51,56,61,63,65,71,74	P	Digital ground, tie to digital ground plane
AVDD	3,10,12,80,83,91,92,93,99	P	Analog power supply, tie to 3.3V
AVSS	7,11,79,85,89,94,95,98,100		Analog ground, tie to analog ground plane
ADVDD3.3	15,76	P	Digital power supply for analog component, tie to 3.3V
AVDD1.8	90	P	Digital power supply for analog component, tie to 1.8V
Others			
NC	1,2,4,5,6,8,9,13,14,20,21,49,50,53,54,57,58,59,77,78,84		Not Connected

Table 1: Pin Description

Electrical Characteristic

Recommended Operating Condition

Symbol	Description	Min	Typical	Max	Unit
T _j	Chip Junction Temperature	-	-	125	°C
VDD1.8	1.8V Digital Core Power Supply Voltage	1.62	1.8	1.98	Volt
AVDD	3.3V Analog Power Supply Voltage	3.15	3.3	3.45	Volt
VDD3.3	3.3V Digital IO Power Supply Voltage	3	3.3	3.6	Volt
AVDD1.8	1.8V Analog Power Supply Voltage	1.7	1.8	1.9	Volt
V _{IH}	Digital Input High Voltage	3	3.3	3.6	Volt
V _{IL}	Digital Input Low Voltage	-	0	-	Volt

Table 2: Recommend Operating Condition

Typical Current and Power Dissipation (ASTC Mode)

Symbol	Description	Typical	Unit
I_VDD1.8	1.8V Digital Core Power Supply Current	350	mA
I_AVDD	3.3V Analog Power Supply Current	70	mA
I_VDD3.3	3.3V Digital I/O Power Supply Current	16	mA
I_AVDD1.8	1.8V Analog Power Supply Current	2	mA
P_VDD1.8	1.8V Digital Core Power Dissipation	630	mW
P_AVDD	3.3V Analog Power Dissipation	231	mW
P_VDD3.3	3.3V Digital IO Power Dissipation	52.8	mW
P_AVDD1.8	1.8V Analog Power Dissipation	3.6	mW
P_Total	Total Power Dissipation	917.4	mW
P_Sleep	Total Power Dissipation (Sleep Mode)	130	mW

Table 3: Typical Current and Power Dissipation (ATSC Mode)

Typical Current and Power Dissipation (QAM Mode)

Symbol	Description	Typical	Unit
I_VDD1.8	1.8V Digital Core Power Supply Current	175	mA
I_AVDD	3.3V Analog Power Supply Current	70	mA
I_VDD3.3	3.3V Digital I/O Power Supply Current	19	mA
I_AVDD1.8	1.8V Analog Power Supply Current	2	mA
P_VDD1.8	1.8V Digital Core Power Dissipation	315	mW
P_AVDD	3.3V Analog Power Dissipation	231	mW
P_VDD3.3	3.3V Digital I/O Power Dissipation	62.7	mW
P_AVDD1.8	1.8V Analog Power Dissipation	3.6	mW
P_Total	Total Power Dissipation	612.3	mW
P_Sleep	Total Power Dissipation (Sleep Mode)	130	mW

Table 4: Typical Current and Power Dissipation (QAM Mode)



MTK

MT8293

Specifications are subject to change without notice.

HDMI PanelLink Cinema Receiver

MT8293 is a low-cost, fully HDMI-compliant receiver that fits directly into home theater products such as LCD TVs, plasma TVs and HDTVs. The receiver is capable of supporting bandwidths up to 165MHz and video resolutions up to 1080p and UXGA. The MT8293 supports the DVD-Audio standard, including 7.1- surround audio at 96kHz and stereo audio at 192kHz.

The built-in High-bandwidth Digital Content Protection (HDCP) decryption engine secures the digital link for transmission of valuable high-definition video and audio. Built-in HDCP self-test engine simplifies manufacturing testing.

FEATHRES

■ Industry-Standard

- HDMI 1.1
- DVI 1.0
- EIA/CEA-861B
- HDCP 1.1

■ Digital Video Output

- Integrated PanelLink Core
- Supports DTV (480i/576i/480p/576p/720p/1080i/1080p) and PC (VGA/XGA/SXGA/UXGA) resolution up to 165MHz (using dual edge to transmit video data for pixel clock over 112MHz)
- Flexible digital video interface
 - 24-bit RGB/YCbCr 4:4:4
 - 16-bit YCbCr 4:2:2
 - 8-bit YCbCr 4:2:2 (ITU-R BT.656)
- Integrated RGB <-> YCbCr color space conversion (both 601 and 709)
- 4:2:2 <-> 4:4:4 converter
- Integrated Deinterlacer for 480i/576i (SDTV only)
- Integrated Down-Scaler (with CEN)

■ Digital Audio Output

- Industry-standard S/PDIF and 3-wire output

- Supports high-end audio including DVD-Audio
 - 2-ch. 32-192kHz or
 - 8-ch. 32-96kHz
- Programmable 3-wire output supports numerous low-cost I2S audio DACs
- Supports IEC60958 2-channel PCM
- Capable of carrying IEC61937 compressed audio (Dolby Digital, DTS, etc.)

■ Content Protection

- Integrated HDCP cipher engine
- External EEPROM for encrypt HDCP keys
- Built-in HDCP self-test
- Decrypts both video and audio

■ System Operation

- Register-programmable via slave I2C interface
- Auto video mode
- Auto audio mode
- Flexible interrupt registers with interrupt pin

■ Power Management

- 1.8V core provides low-power operation
- Flexible power-down modes

■ Outline

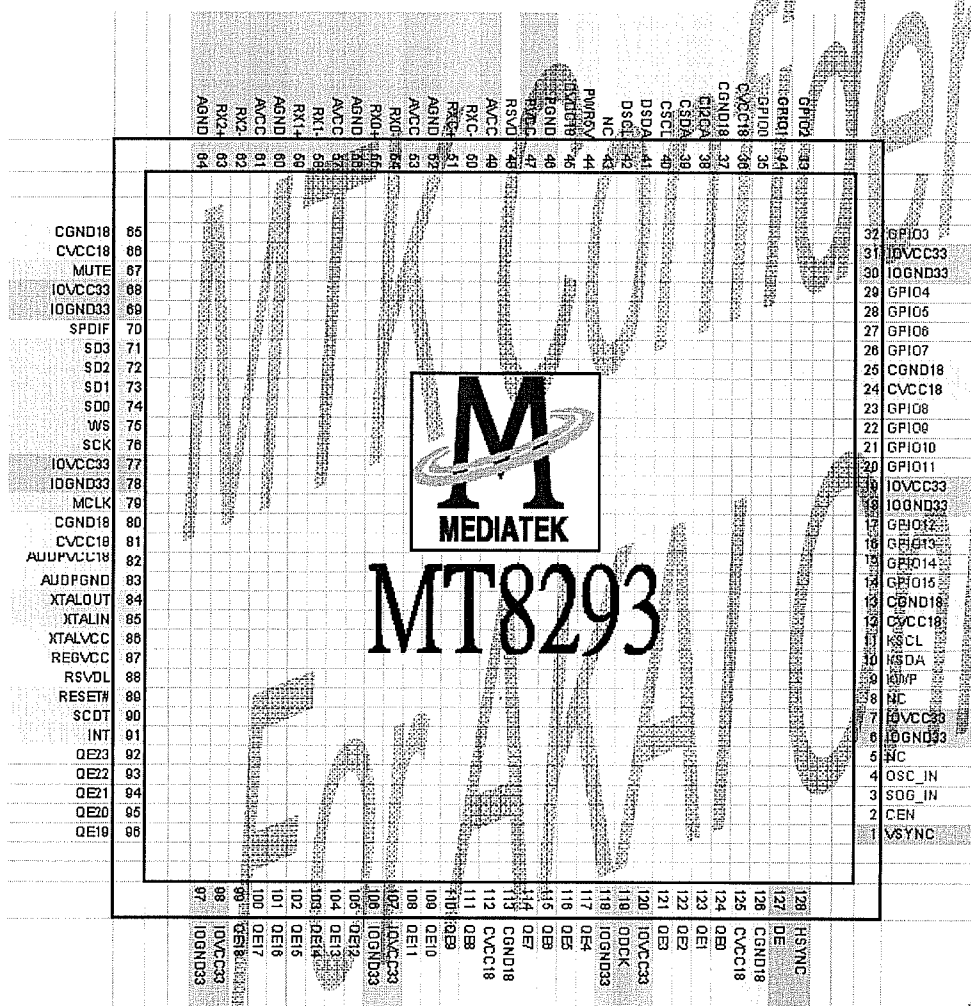
- 128-pin QFP package

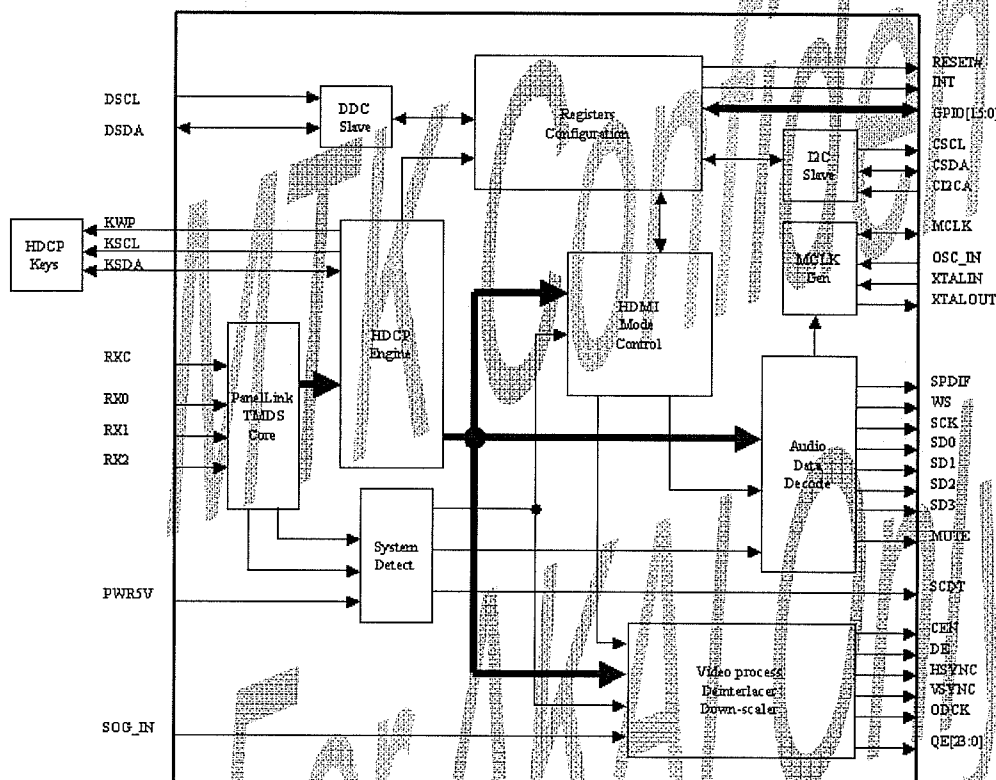


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Item	Symbol	Pin #	Type	Description
DIGITAL				
Power/Ground (45)				
1	CVCC18	12,24,36,45,66,81,112,125	I	Digital Logic 1.8V power
2	CGND18	13,25,37,65,80,113,126	I	Digital Logic ground
3	IOVCC33	7,19,31,68,77,98,107,120	I	Input/Output Pin 3.3V power
4	IOGND33	6,18,30,69,78,97,106,118	I	Input/Output Pin ground
5	AVCC	49,53,57,61	I	TMDS Analog 3.3V power
6	AGND	52,56,60,64	I	TMDS Analog ground
7	PVCC	47	I	TMDS PLL 3.3V power
8	PGND	46	I	TMDS PLL ground
9	AUDPVCC18	82	I	ACR PLL 1.8V power
10	AUDPGND	83	I	ACR PLL ground
11	XTALVCC	86	I	ACR PLL crystal input 3.3V power
12	REGVCC	87	I	ACR PLL regulator 3.3V power
Configuration/Programming (20)				
1	INT	91	O	Interrupt output
2	RESET#	89	I	Reset Pin. Active low
3	DSCL	42	I	DDC I2C clock, 5V tolerance
4	DSDA	41	I/O	DDC I2C data, 5V tolerance
5	CSCL	40	I	Configuration I2C clock
6	CSDA	39	I/O	Configuration I2C data
7	KSCL	11	O	KEYS EEPROM I2C clock
8	KSDA	10	I/O	KEYS EEPROM I2C data
9	KWP	9	O	KEYS EEPROM write protect
10	SCDT	90	O	Indicates active video at HDMI input port
11	CISCA	38	I	I2C device address select

Item	Symbol	Pin #	Type	Description
12	PWR5V	44	I	TMDS port transmitter detect (hot plug), 5V tolerance
13	RSVDL	88	I	Must be tied low
14	RSVD	48	O	
15	NC	43	-	No connect
16	NC	8,5	-	No connect
17	OSC_IN	4	I	Oscillator input, External in
18	SOG_IN	3	I	SOG input, External AD in
19	CEN	2	O	Clock enable, for 8202 CEN input
Digital Audio Interface (9)				
1	MCLK	79	I/O	Audio master clock input reference
2	SCK	76	O	I2S serial clock output
3	WS	75	O	I2S word select output
4	SD0	74	O	I2S serial data output
5	SD1	73	O	I2S serial data output
6	SD2	72	O	I2S serial data output
7	SD3	71	O	I2S serial data output
8	SPDIF	70	O	S/PDIF audio output
9	MUTE	67	O	Mute audio output
GPIO Interface (16)				
1	GPIO0	35	I/O	GPIO
2	GPIO1	34	I/O	GPIO
3	GPIO2	33	I/O	GPIO

Item	Symbol	Pin #	Type	Description
4	GPIO3	32	I/O	GPIO
5	GPIO4	29	I/O	GPIO
6	GPIO5	28	I/O	GPIO
7	GPIO6	27	I/O	GPIO
8	GPIO7	26	I/O	GPIO
9	GPIO8	23	I/O	GPIO
10	GPIO9	22	I/O	GPIO
11	GPIO10	21	I/O	GPIO
12	GPIO11	20	I/O	GPIO
13	GPIO12	17	I/O	GPIO
14	GPIO13	16	I/O	GPIO
15	GPIO14	15	I/O	GPIO
16	GPIO15	14	I/O	GPIO
TTL Interface (28)				
1	DE	127	O	Data enable
2	VSYNC	1	O	Vertical sync
3	HSYNC	128	O	Horizontal sync
4	ODCK	119	O	Output data clock
5	QE0	124	O	24-bit Even pixel
6	QE1	123	O	24-bit Even pixel
7	QE2	122	O	24-bit Even pixel



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Item	Symbol	Pin #	Type	Description
8	QE3	121	O	24-bit Even pixel
9	QE4	117	O	24-bit Even pixel
10	QE5	116	O	24-bit Even pixel
11	QE6	115	O	24-bit Even pixel
12	QE7	114	O	24-bit Even pixel
13	QE8	111	O	24-bit Even pixel
14	QE9	110	O	24-bit Even pixel
15	QE10	109	O	24-bit Even pixel
16	QE11	108	O	24-bit Even pixel
17	QE12	105	O	24-bit Even pixel
18	QE13	104	O	24-bit Even pixel
19	QE14	103	O	24-bit Even pixel
20	QE15	102	O	24-bit Even pixel
21	QE16	101	O	24-bit Even pixel
22	QE17	100	O	24-bit Even pixel
23	QE18	99	O	24-bit Even pixel
24	QE19	96	O	24-bit Even pixel
25	QE20	95	O	24-bit Even pixel
26	QE21	9	O	24-bit Even pixel
27	QE22	93	O	24-bit Even pixel
28	QE23	92	O	24-bit Even pixel



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Item	Symbol	Pin #	Type	Description
ANALOG (8)				
Differential signal				
1	RXC+	51	I	TMDS input clock pair
1	RXC-	50	I	TMDS input clock pair
1	RX0	55	I	TMDS input data pair
1	RX0	54	I	TMDS input data pair
1	RX1	59	I	TMDS input data pair
1	RX1	58	I	TMDS input data pair
1	RX2	63	I	TMDS input data pair
1	RX2	62	I	TMDS input data pair
PLL group(2)				
68	XTALIN	85	I	Crystal input PAD
69	XTALOUT	84	O	Crystal output PAD

**MTK****MT8202**

Specifications are subject to change without notice.

HDTV-Ready LCD TV Chip

MT8202 is a highly integrated single chip for LCD TV supporting video input and output format up to HDTV. It includes 3D comb filter TV decoder to retrieve the best image from popular composite signals. Embedded HDTV/VGA decoders let the high bandwidth input signals perfectly reproduced. 24/16/8 bits digital port may accept all kinds of external digital input video source. New 2nd generation advanced motion adaptive de-interlacer converts accordingly the interlace video into progressive one with overlay of a 2D Graphic processor. Advanced full function color processing with fully 10-bit path provides high quality video contents. Independent two Flexible scalers provide wide adoption to various LCD panels for two of different video sources at the same time. Its on-chip audio processor decodes analog signals from tuner with lip sync control, delivering high quality post-processed sound effect to customers. On-chip microprocessor reduces the system BOM and shortens the schedule of UI design by high level C program. MT8202 is a cost-effective and high performance HDTV-ready solution to LCD TV manufactures.

FEATURES

■ Video Input

- Support fully programmable 8 Composite/SV input pins
- Support 2 Component inputs with SDTV format & HDTV 480p/720p/1080i format
- Support 1 VGA input up to SXGA (1280x1024x75Hz) including SOG signals
- Support DVI 24-bit RGB digital input
- Support CCIR-656/601 digital input

■ TV decoder

- Full 10-bit data path to enhance the video resolution and reduce digital truncation errors
- Support PAL (B, G, D, H, M, N, I, Nc), PAL (Nc), PAL, NTSC, NTSC-4.43, SECAM
- Automatic Luma/Chroma gain control

- Automatic TV standard detection
- 2nd generation NTSC/PAL Motion Adaptive 3D comb filter with huge improvement
- Motion Adaptive 3D Noise Reduction
- VBI decoder for Closed-Caption/XDS/Teletext/WSS/VPS
- High speed advanced Teletext/Closed-Caption drawing engine directly on OSD plane
- Macrovision detection
- Adjustable horizontal delay for combination of SCART Composite/RGB input

■ Video Processor

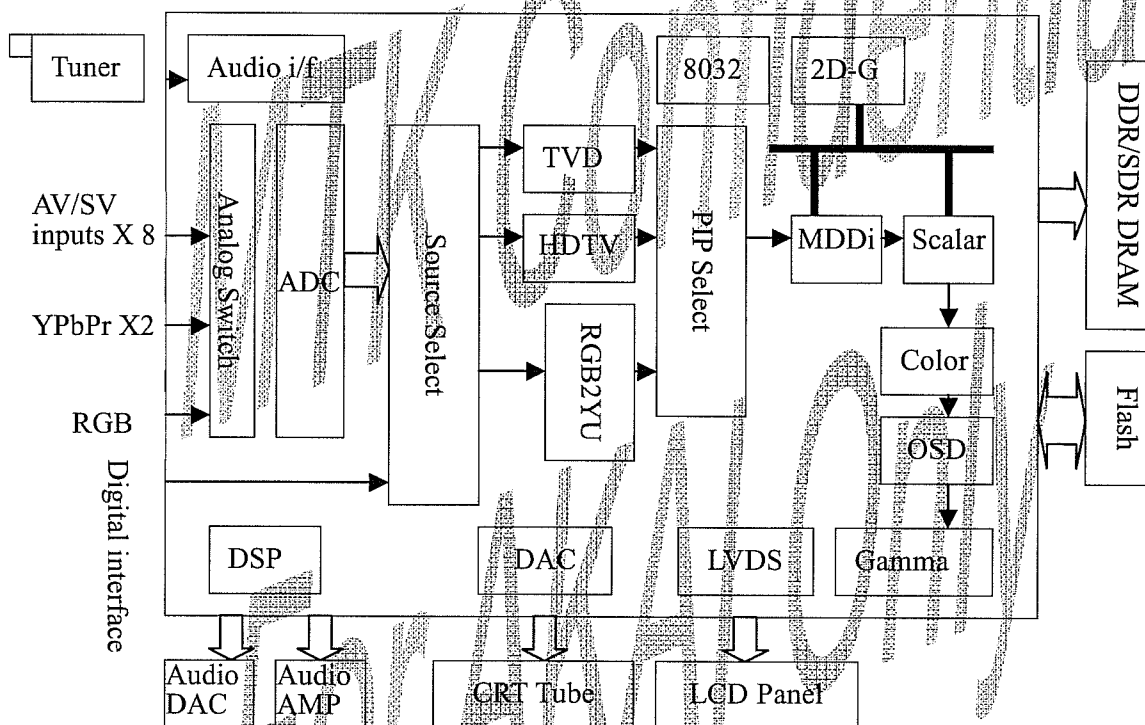
- Fully 10-bit processing to enhance the video quality
- Advanced flesh tone and color processing
- Gamma/anti-Gamma correction
- Advanced Color Transient Improvement (CTI)
- 2D Peaking
- Advanced horizontal/vertical sharpness
- Saturation/hue adjustment
- Brightness and contrast adjustment
- Black level extender
- White peak level limiter
- Adaptive Luma/Chroma management
- Automatic detect film or video source
- 3:2/2:2 pull down source detection
- 2nd generation Advanced Motion adaptive de-interlacing
- Arbitrary ratio vertical/horizontal scaling of video, from 1/32X to 32X
- Advanced linear and non-linear Panorama scaling
- Programmable Zoom viewer
- Progressive scan output
- Picture-in-Picture (PIP)
- Picture-Out-Picture (POP)
- Advanced dithering processing for LCD display with 6/8/10 bit output
- Frame rate conversion, 50Hz to 75Hz

■ Audio DSP

- Support BTSC/EIAJ/A2/NICAM decode
- Stereo demodulation, SAP demodulation

- Noise reduction
- Mode selection (Main/SAP/Stereo)
- Pink noise and white noise generator
- Equalizer
- Sub-woofer/Bass enhancement
- Noise auto mute
- 3D surround processing include virtual surround
- Audio and video lip synchronization
- Support Reverberation
- Audio Input/Output
 - Decode audio AF from Tuner
 - 2 channel audio L/R digital line in
 - 7.1-channel slave digital line in
 - Including full 7.1-channels digital output, 2-channel bypass and 2-channel headphone output
 - Embedded 3 internal DAC output
- DRAM Controller
 - Supports up to 32M-byte SDR/DDR DRAM
 - Supports 2x16 bit SDR/DDR bus interfaces
 - Build in a DRAM interface programmable clock to optimize the DRAM performance
 - Programmable DRAM access cycle and refresh cycle timings
 - Support 3.3/2.5-Volt SDR/DDR interface
- Video Output
 - TV pattern generator for testing
 - Interlaced 50Hz to 120Hz
 - Support up to 1366 horizontal points
 - 6/8/10-bit single channel or 6/8/10-bit dual channel LVDS output
 - Support video output mirror and upside down
- 2D-Graphic/3 OSD processor
 - Embedded Two backend RGB domain OSD planes and one YUV domain OSD
 - Support Text/Bitmap decoder
 - Support line/rectangle/gradient fill
 - Support bitblt
 - Support color Key function
 - Support Clip Mask
 - Support Alpha blending with video output
 - 65535/256/16/4/2-color bitmap format OSD,
 - Automatic vertical scrolling of OSD image
 - Support OSD mirror and upside down
- Host Micro controller
 - Turbo 8032 micro controller
 - Built-in internal 373 and 8-bit programmable lower address port
 - 2048-bytes on-chip RAM
 - Up to 4M bytes FLASH-programming interface
 - Supports 5/3.3-Volt FLASH interface
 - Supports power-down mode
 - Supports additional serial port
 - IR control serial input
 - Support 2 RS232 interface for external source communication
 - Support 2 PWM output
 - Support DDC2Bi/DDC2B/DDC1/DDCCI
 - Programmable GPIO setting for complex external device control
- Outline
 - 388-pin BGA package
 - Lead Free
 - 3.3/2.5/1.8-Volt operating voltages
 - 0.18um process

BLOCK DIGRAM



Analog Switch

Analog switches are built in MI8202 to connect to 17 input signals and there is need to add external components to add analog video multiplexes on board.

There are 9 high-speed differential input pairs for 3 sets of YPRPB/VGA input signals.

The 8 Composite/S signal input pins can be fully programmed to connect to any AV/SV inputs.

ADC/ Source Select

The video ADC sample analog input signals. After ADC, all signal processing is digital domain. The source select multiplex all inputs from digital and analog video ports and route them into data path.

Audio Interface

Audio interface accept analog audio signal from Tuner, e.g. AF. It also includes preprocessing circuit to filter the noisy audio signals. Audio decoder will decode the BTSC or NICAM, and output best sound with enhanced 3D surround post-processing.

Embedded 7.1 channel digital audio input (slave) and 2-channels (master) digital audio inputs.

Embedded 3 high performance audio DACs

DSP



DSP handle audio decoding as well as computing intensive jobs. The downloadable micro code enables fast function convergence for various audio standards in the world.

Advanced DSP engine supports full functions of sound effects.

MDDi/Scaler

MDDi is MTK proprietary de-interlacing technology. 2nd generation MDDi solution provides improved low angle processing and more accurate motion detection for all interlace sources. The techniques reduce jagged edges and broken images. The MDDi engine supports both Main and Sub channel SDTV inputs or one channel 1080i high quality de-interlacing.

Two totally independent scaler support full functions of PIP/POP and frame rate conversion.

With MDDi and high quality scaler, MT8202 guarantee all input format could be translated to output format with best video quality for motion and still pictures.

Color/Gamma

MT8202 includes advanced color management function to allow user to improve video quality with fully flexibility. With contrast/hue/saturation/Gamma/anti-Gamma/flesh tone function, MT8202 deliver the best video quality with vivid color.

Advanced dither function support 6/8/10-bit video output for any kinds of display unit (LCD, PDP, CRT).

8032

On-chip Turbo8032 provide the most cost effective development environment for system house. Well-proven F/W could speed up the system design significantly.

2D-G/OSD

On-chip graphic engine draw bitmap OSD and store them into DRAM. OSD read data from DRAM and display on screen. With 2D-G and OSD. The computing power requirement of μP will be minimized.

One YUV space OSD added to support Main/PIP Teletext/Close-caption functions.



MTK



MT5351

Specifications are subject to change without notice.

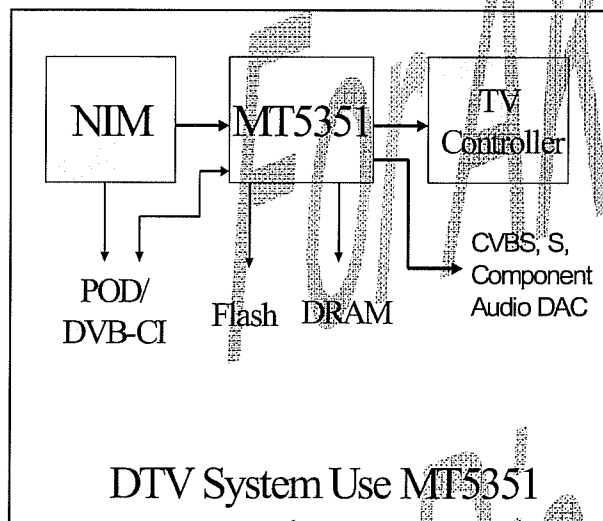
DTV Backend Decoder SOC

MediaTek MT5351 is a DTV Backend Decoder SOC which support flexible transport demux, HD MPEG-2 video decoder, JPEG decoder, MPEG1,2, MP3, AC3 audio decoder, HD TV encoder. The MT5351 enables consumer electronics manufactures to build high quality, feature-rich DTV, STB or other home entertainment audio/video device.

World-Leading Technology: HW support worldwide major broadcast network and CA standards, include ATSC, DVB, OpenCable, DirectTV, MHP.

Rich Feature for high value product: To enrich the feature of DTV, the MT5351 support 1394-5C component to external DVHS. Dual display, PIP/POP and quad pictures provide user a whole new viewing experience.

Credible Audio/Video Quality: The MT5351 use advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback. The embedded 4X over-sample video DAC could generate very fine display quality. Also, the audio 3D surround and equalizer provide professional entertainment



Key Features:

1. Flexible Demuxer
2. Dual HD MPEG2 Video Decoder
3. Dual MPEG1,2, MP3, AC3 Audio decode
4. Dual Display
5. PIP/POP/Quad Mode
6. IEEE1394-5C
7. POD/DVB-CI

Application:

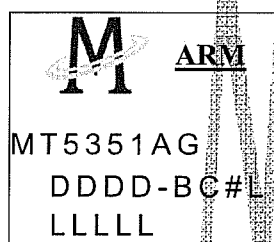
1. DTV
2. Set-top Box
3. DTV Recorder
4. Home Media Center

Order Information:

MT5351AG → one HD decoder

MT5351CG → two HD decoder

All Package are Lead Free



IC Top View:

DDDD: Date Code
#: Subcontractor Code
LLLLL: Lot Number

General Feature List

- Host CPU
 - ARM 926EJ
 - 16K I-Cache and 16K D-Cache
 - 8K Data TCM and 8K Instruction TCM
 - JTAG ICE interface
 - Watch Dog timers
- Transport Demuxer
 - Support 3 independent transport stream inputs
 - Support serial / parallel interface for each transport stream input.
 - Support ATSC, DVB, and MPEG2 transport stream inputs
 - Programmable sync detection.
 - Support DES/3-DES de-scramble
 - 96 PID filter and 128 section filters.
 - Support TS recording via IEEE1394 interface
- MPEG2 Decoder
 - Support dual MPEG-2 HD decoder or up to 8 SD decoder
 - Complaint to MP@ML, MP@HL and MPEG-1 video standards
- JPEG Decoder
 - Decode Base-line or progressive JPEG file
- 2D Graphics
 - Support multiple color modes
 - Point, horizontal/vertical line primitive drawing
 - Rectangle fill and gradient fill functions
 - Bitblt with transparent, alpha blending, alpha composition and stretch
 - Font rendering by color expansion
 - Support clip masks
 - YCbCr to RGB color space transfer
- OSD Display
 - 3 linking list OSDs with multiple color mode
 - OSD scaling with arbitrary ratio from 1/2x to 2x
 - Square size, 32x32 or 64x64 pixel, hardware cursor
- Video Processing
 - Advanced Motion adaptive de-interlace on SDTV resolution
- Support clip
- 3:2:2 pull down source detection
- Arbitrary ratio vertical/horizontal scaling of video, from 1/15X to 16X
- Support Edge preserve
- Support horizontal edge enhancement
- Support Quad-Picture
- Main Display
 - Mixing two video and three OSD and hardware cursor
 - Contrast/Brightness adjustment
 - Gamma correction
 - Picture-in-Picture (PIP)
 - Picture-Out Picture (POP)
 - 480i/576i/480p/576p/720p/1080i output
- Auxiliary Display
 - Mixing one video and one OSD
 - 480i/576i output
- TV Encoder
 - Support NTSC M/N, PAL M/N/B/D/G/H/I
 - Macrovision Rev 7.1.L1
 - CGMS/WSS
 - Closed Captioning
 - Six 12-bit video DACs for CVBS, S-video or RGB/YPbPr output
- Digital Video Interface
 - Support SAV/EAV
 - Support 8/16 for SD/HD digital video input
 - Support 8/16/24 bits digital output for main display
 - Support 8 bits digital output for aux display
- DRAM Controller
 - Supports 64Mb to 1Gb DDR DRAM devices
 - Configurable 32/64 bit data bus interface
 - Support DDR266, DDR333, DDR400 JEDEC specification compliant SDRAM
- Peripheral Bus Interface
 - Support NOR/NAND flash
 - Support CableCard host control bus
- Audio

- Support Dolby Digital AC-3 decoding
- MPEG-1 layer I/II, MP3 decoding
- Dolby prologic II
- Main audio output: 5.1ch + 2ch (down mix)
- Auxiliary audio output: 2ch
- Pink noise and white noise generator
- Equalizer
- Bass management
- 3D surround processing include virtual surround
- Audio and video lip synchronization
- Support reverberation
- SPDIF out
- I2S I/F

■ Peripherals

- Three UARTs with Tx and Rx FIFO, two of them have hardware flow control
- Two serial interfaces, one is master only, the other can be set to master mode or slave mode
- Two PWMs
- IR blaster and receiver
- IEEE 1394 link controller
- IDE bus: ATA/ATAPI7 UDMA mode 5, 100 MB/s
- Real-time clock and watchdog controller
- Memory card I/F: MS/MS-Pro, SD, CF, and MMC
- PCMCIA/POD/CI interface

■ IC Outline

- 471 Pin BGA Package
- 3.3V/1.2V dual Voltage

Electrical Characteristics

Absolute Maximum Rating

Symbol	Parameters	Value	Unit
IOVDD	3.3V supply voltage	-0.5 to 4.6	V
CVDD	1.2V supply voltage	-0.5 to 1.8	V
AVDD	Analog supply voltage	-0.5 to 4.6	V
RVDD	DDR supply voltage	-0.5 to 3.5	V
VIN(3.3V)	Input Voltage(3.3V IO)	VSS-1.0 to 3.63	V
VIN(5V tolerance)	Input Voltage(5V tolerance IO)	VSS-1.0 to 5.5	V
Vout	Output Voltage	-0.3 to VDD3+0.3	V
Ts	Storage Temperature	-40 to 150	C
Ta	Ambient Temperature	0 to 70	C

DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
IOVDD	3.3V supply voltage	2.97	3.3	3.63	V
CVDD	1.2V supply voltage	1.08	1.2	1.32	V
AVDD	Analog supply voltage	2.97	3.3	3.63	V
VIH(3.3V)	3.3V input voltage high	2.0			V
VIL(3.3V)	3.3V input voltage low			0.8	V
VOH(3.3V)	3.3V output voltage high	2.4			V
VOL(3.3V)	3.3V output voltage low			0.4	V
VIH(3/5V)	3/5V tolerance input voltage high	2.0			V
VIL(3/5V)	3/5V tolerance input voltage low			0.8	V
VOH(3/5V)	3/5V tolerance output voltage high	2.4			V
VOL(3/5V)	3/5V tolerance output voltage low			0.4	V
Tj	Junction operation temperature	-40	25	125	C
PD(estimate)	Power dissipation		1.5		W
Pdown	Power down mode		2		mW

DDR ELECTRICAL Characteristics and DC Operating Condition

Symbol	Parameters	Min	Typ	Max	Unit
RVDD(DDR333)	DDR I/O supply voltage for DDR266 or DDR333	2.3	2.5	2.7	V
RVDD(DDR400)	DDR I/O supply voltage for DDR400	2.5	2.6	2.7	V
DVREF	DDR I/O reference voltage	0.49*RVDD	0.5*RVDD	0.51*RVDD	V
VTT	DDR I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V
VIH	DDR input voltage high	VREF+0.15		RVDD+0.3	V
VIL	DDR input voltage low	-0.3		VREF-0.15	V

DDR AC Operating Condition

Symbol	Parameters	Min	Typ	Max	Unit
VIH	Input high voltage, DQ, DQS	DVREF+0.31			V
VIL	Input low voltage, DQ, DQS			DVREF-0.31	V
Vslew	Input minimum slew rate	1.0			V/ns
Vswing	Input maximum swing			1.5	V

Digital Power Amplifier R2S15102NP

10Wx2ch(SE)/20Wx1ch(BTL) Digital Audio Power Amplifier

1.Outline

R2S15102NP is a Digital Power Amplifier IC developed for TV.

R2S15102NP can realize maximum Power 10W × 2ch

(VD = 24V, THD = 10%, SE) at 8 Ω load.

It is possible to replace from the conventional analog amplifier system to the digital amplifier system easily.

2.Feature

High Output Power(THD=10%)without external Heat Sink

(note) the thermal pad is soldered the thermal pad with the printed-circuit board directly.

Recommended Power Condition

SE operation mode :10Wx2ch(VD=24V) at 8 Ω

BTL operation mode: 20Wx1ch(VD=18V) at 8 Ω

The RENESAS original circuits realize high power efficiency, low noise and low distortion characteristics.

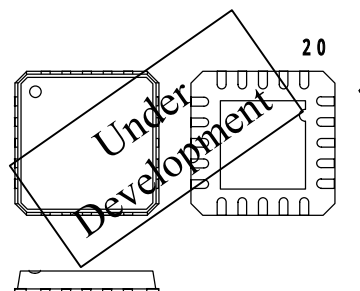
Pop sound Less

Built-in protection function

(Over Current, Over Temperature and Under Voltage)

Built-in Mute and Stand-by function

Fig. 1 Package



20pin QFN

Body : 6 x 6 mm

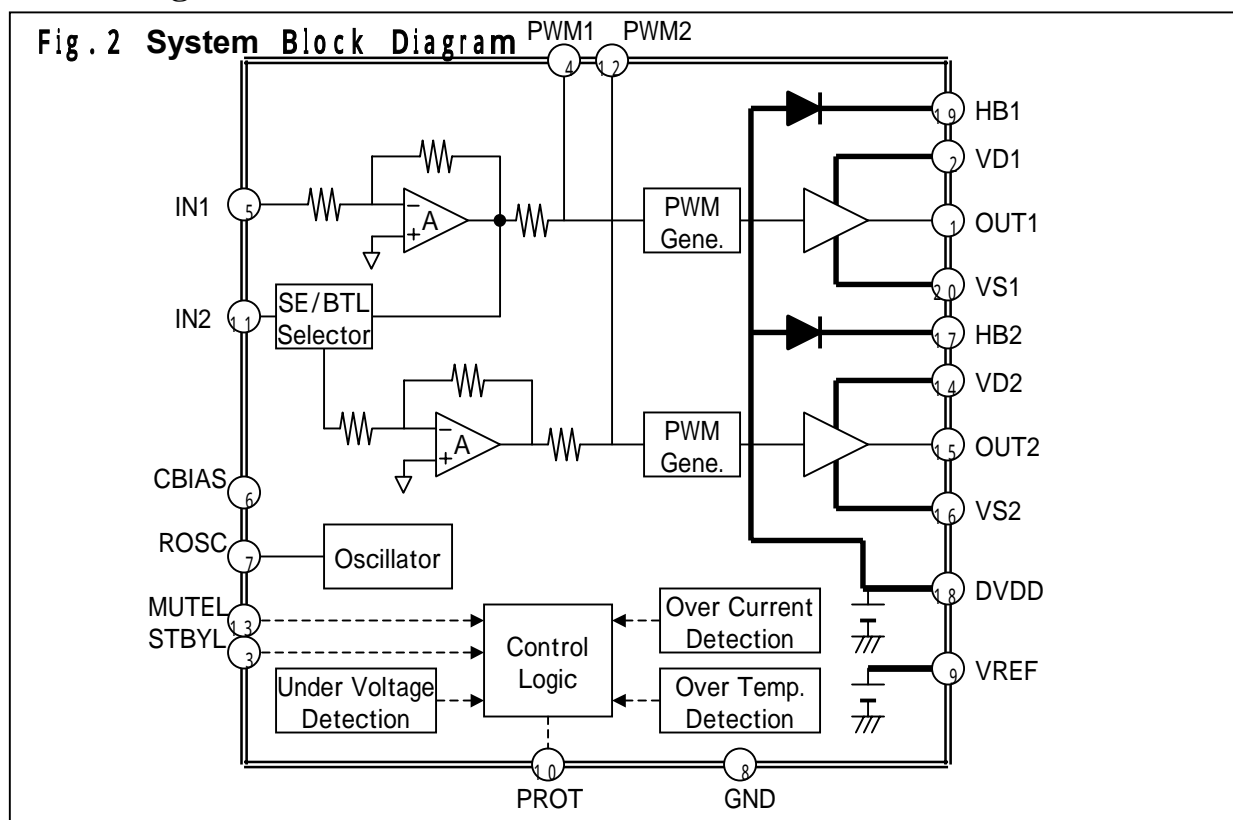
Lead pitch : 0.8 mm

3.Operating Condition

Recommended Power supply voltage : from 11V to 25V

Recommended Speaker Impedance : from 4 to 8Ω

4.Block Diagram



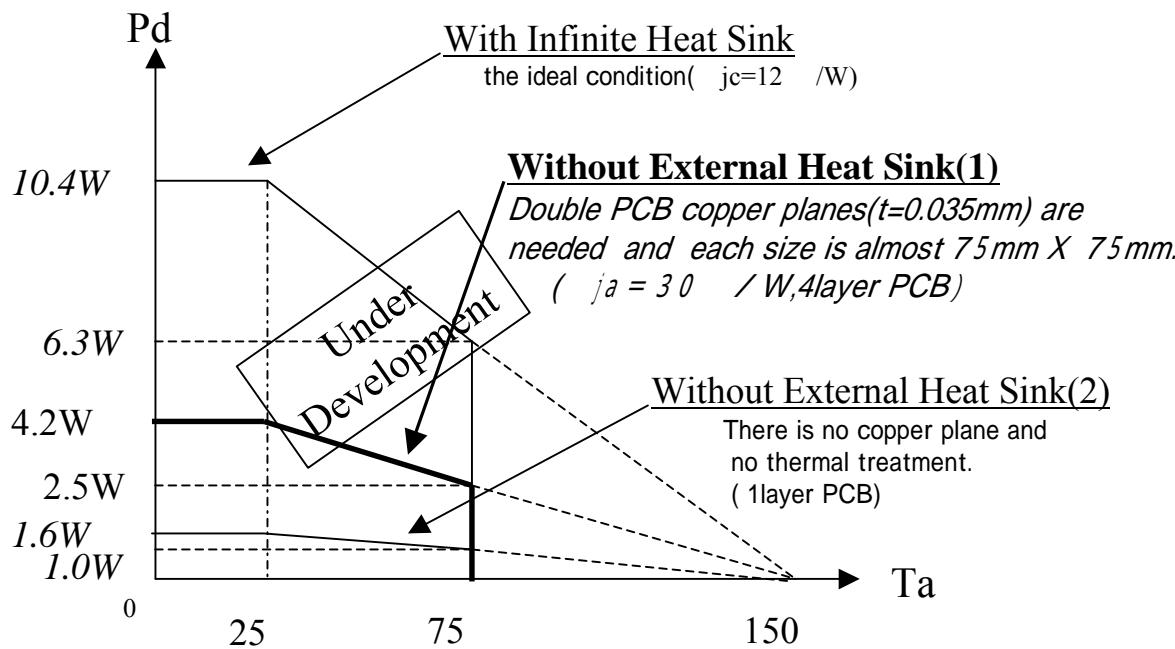
5 . Pin Configuration(Table.1)

No.	NAME	I/O	Description	
1	OUT1	O	Power Output pin #1	
2	VD1	-	Power supply pin for power output stage #2	
3	STBYL	I	Stand-by control pin. When this is “L”, circuit current is reduced. There is the pull-down resistor: 50Kohm(typ.).	
4	PWM1	I	PWM input pin #1 (for phase compensation)	
5	IN1	I	Analog input #1. The gain is depended on the external resistance .	
6	CBIAS	I/O	A capacitor is connected so that it may not be influenced of power supply change(Ripple Filter).	
7	ROSC	I	Control pin for PWM carrier frequency	
8	GND	-	GND pin for analog block	
9	VREF	I/O	Capacitor connection pin for analog block reference voltage source	
10	PROT	O	Protection Timer pin. At protection mode, the output becomes “L”-level. (The timing capacitor is connected)	
11	IN2	I	SE operation	Analog input #2(as same as IN1)
		I	BTL operation	When this is connected to DVDD pin via the resistor, Reversed signal of OUT1 is output to OUT2.
12	PWM2	I	PWM input pin#2 (for phase compensation)	
13	MUTEL	I	Mute control pin. When this is “L”, it becomes mute status.	
14	VD2	-	Power supply pin for power output stage #2	
15	OUT2	O	Power Output pin #2	
16	VS2	-	Ground pin for power output stage #2	
17	HB2	I/O	Capacitor connection pin for bootstrap	
18	DVDD	O	Built-in power supply pin for internal digital block.	
19	HB1	I/O	Capacitor connection pin for bootstrap #1	
20	VS1	-	Ground pin for power output stage #1	

6 . Absolute Maximum Rating(Table.2)

Symbol	Parameter	Condition	Value	Unit
VD max	Maximum VD Voltage	VD1,VD2 pin voltage	27	V
HB max	Maximum HB Voltage	HB1、 HB2 pin voltage	40	V
Pd	Power dissipation	Ta = 25°C :See Fig.3	4.2	W
ja	Thermal Resistance	See Fig.3	30	/W
Tj	Junction temperature	Maximum Temperature	150	
Ta	Operating ambient temperature	Temperature range	-20 ~ 75	
Tstg	Storage temperature	Temperature range	-40 ~ 150	

Fig.3 Thermal De-rating(on PCB: printed-circuit board):Size 75mm x 75mm

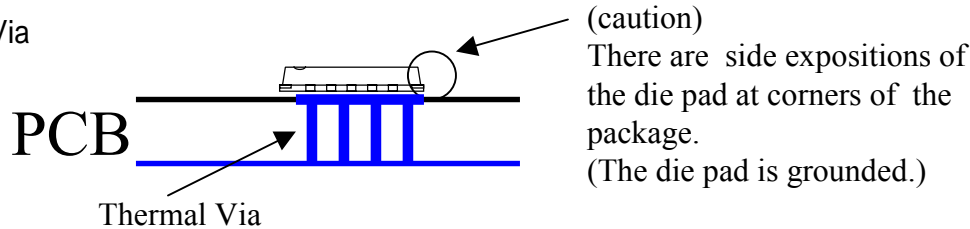


(NOTE)

PCB pattern design for high effective thermal conductivity

(1)The exposed die pad is **directly** soldered with the printed-circuit board pattern .

(2)Thermal Via

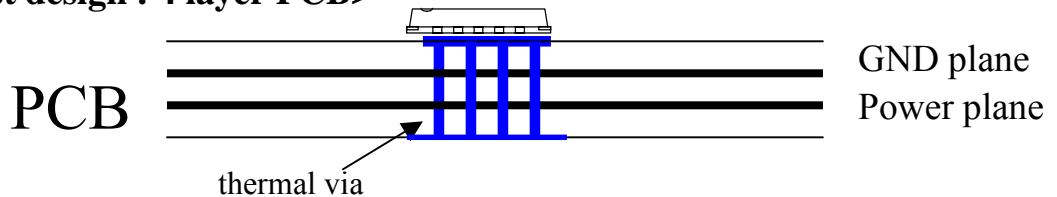


Consideration about the PCB design

The Power dissipation at 10Wx2ch(SE) or 20Wx1ch(BTL) is estimated almost 2W. It has enough margin, designing the PCB at $j_a=30$ /W.

(1)PCB basic design (copper plane)

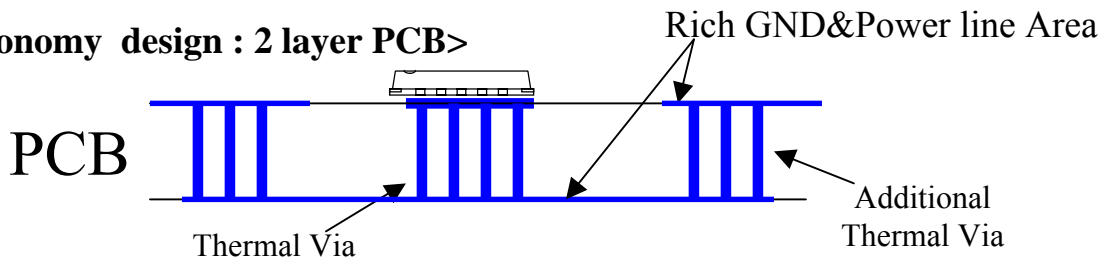
<the best design : 4 layer PCB>



<PCB size estimation >

10Wx2ch: 75mm x 75mm

<the economy design : 2 layer PCB>



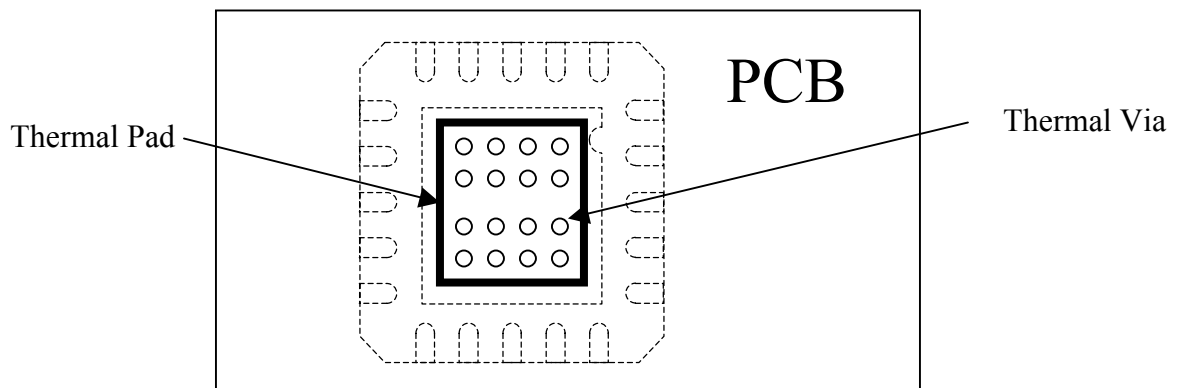
The GND&Power line total area size is also equal to the above GND&Power line total area size of the 4layer PCB.

<PCB size estimation >

10Wx2ch: (75+)mm x (75+) mm

(2)PCB Thermal Pad

The exposed die pad is **directly** soldered with the printed-circuit board pattern .



Digital Power Amplifier R2S15102NP

7 . Recommended Operating condition(Table.3)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VD	Supply Voltage	VD1,VD2 pin voltage	11	-	25	V
VH	Control voltage of high level	STBYL, MUTEL	2	-	5	V
VL	Control voltage of low level	STBYL, MUTEL	0	-	0.8	V
fosc	Carrier Frequency	R= 33k	300	400	600	kHz

- (note)
- STBYL: High level:normal operation Low level:Stand-by
 - MUTEL:High level:normal operation Low level:Mute
 - The carrier frequency can be changed by the resistance at Pin#.7 .

8 . Electronic Characteristics(Table.4)

(Unless otherwise noted, Ta=25°C, VD=24V, Carrier Frequency=400kHz, f=1kHz,SE operation)

Symbol	Parameter		Condition	MIN	TYP	MAX	Unit
IVD	Circuit Current		No Signal	TBD	28	TBD	mA
			MUTE	TBD	-	TBD	mA
			Stand-by	-	-	10	uA
VDPR	Detection Voltage		VD under-voltage	TBD	9.8	TBD	V
TPR	Protection Temperature		Thermal Shut-dawn	-	150	-	
TRL	Release Temperature		Thermal Shut-dawn	-	120	-	
IPR	Protection Current		Output over-current	-	6	-	A
Pomax	Maximum output power	at SE	THD=10%、VD=24V、RL=8	TBD	10	-	W/ch
		at BTL	THD=10%、VD=18V、RL=8	TBD	20	-	W
THD	Total Harmonic Distortion		Po=1W	-	0.1	TBD	%
No	Output Noise level		A-Weighted filter	-	(100)	TBD	uVrms
Eff	Power Efficiency	at SE	Po=10+10W	TBD	93	-	%
		at BTL	Po=20W	TBD	89	-	%
Mute	Mute Attenuation			TBD	80	-	dB
PSRR	Ripple Rejection Ratio		dVD=100mVrms,f=100Hz	TBD	50	-	dB

9 . Application Examples

Fig.4 SE operation mode(10Wx2ch)

(note)

“R for GND” ‘s are for the evaluation only and not needed actually.

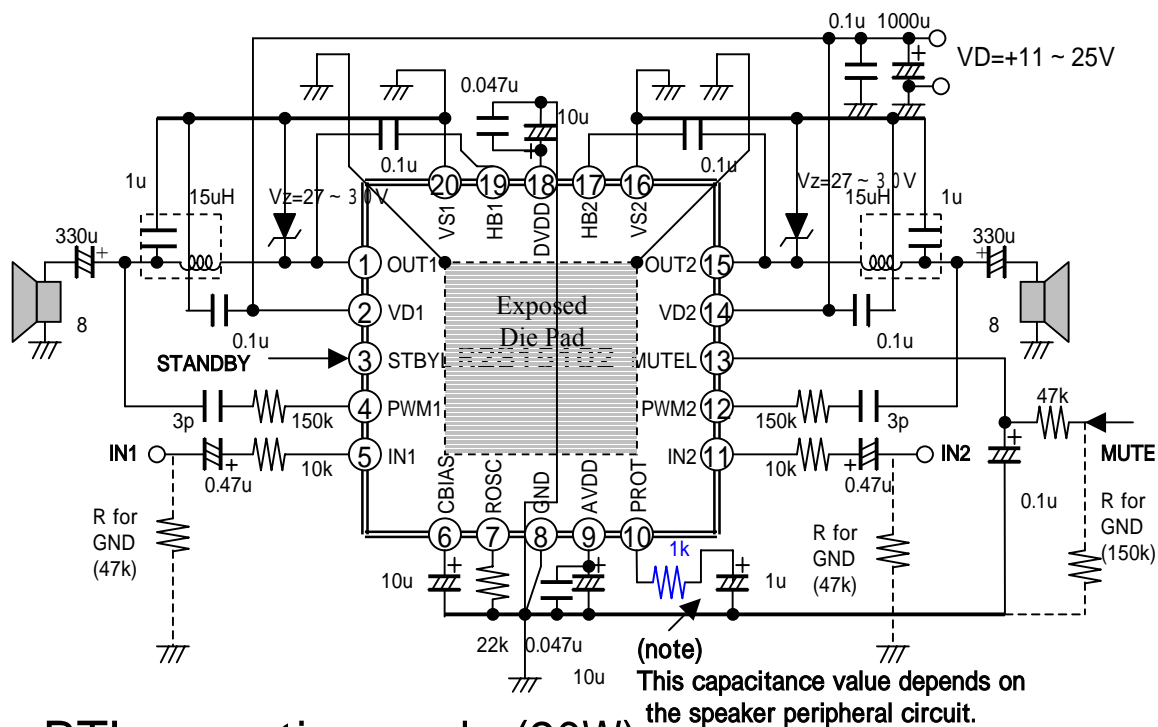
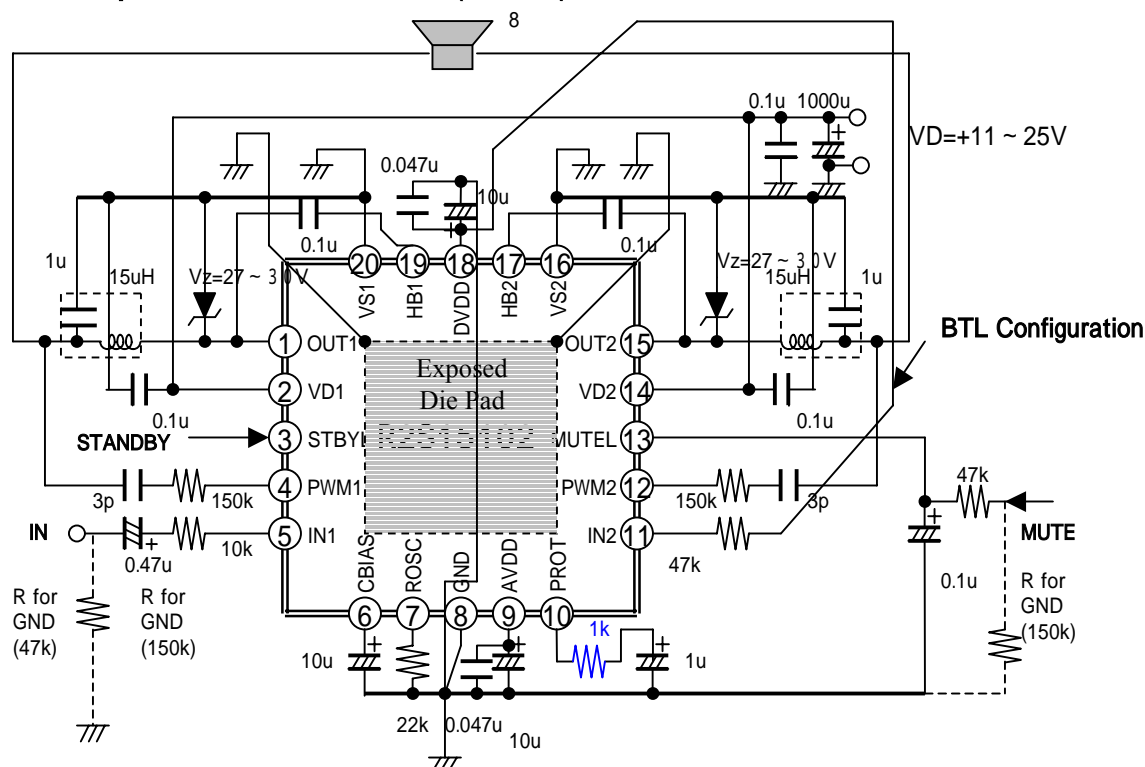


Fig.5 BTL operation mode (20W)



Digital Power Amplifier R2S15102NP

**Fig.6 BTL operation mode(20W)
with PWM direct input**

(note)

“R for GND” ‘s are
for the evaluation only and
not needed actually.

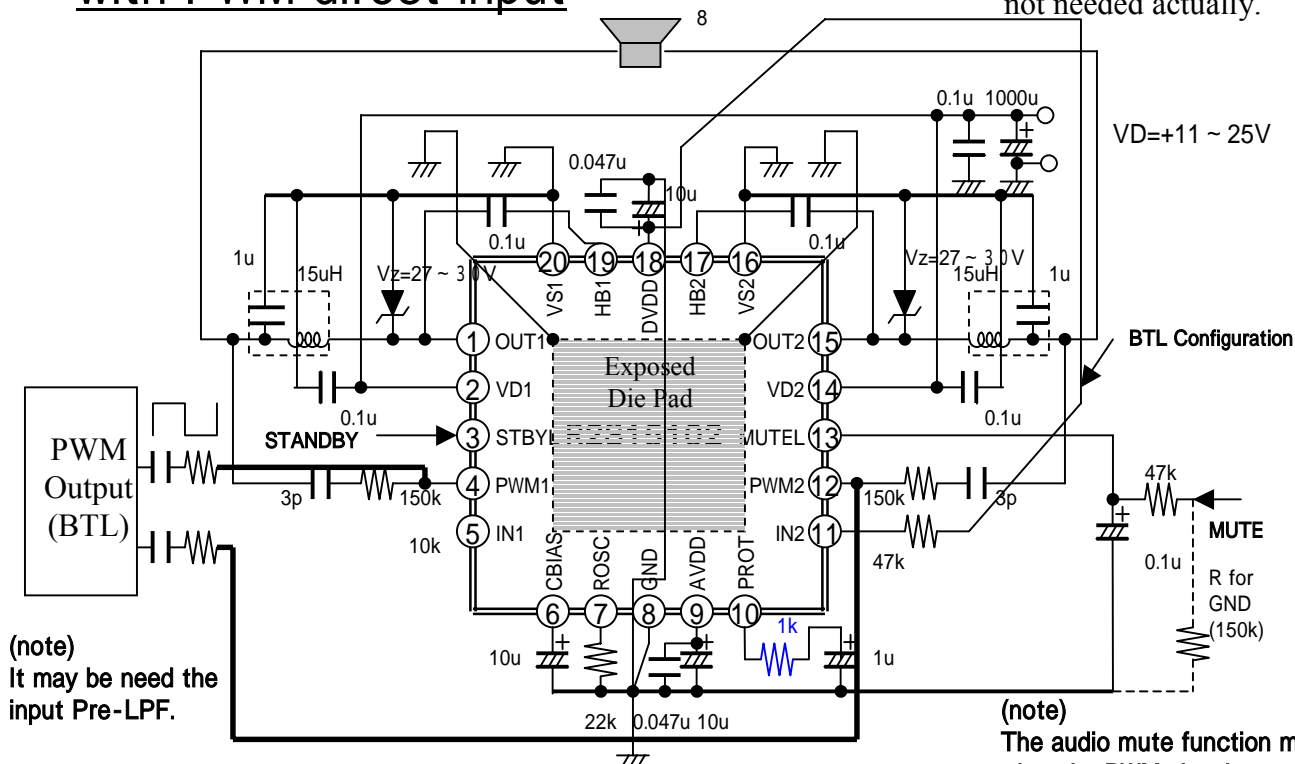
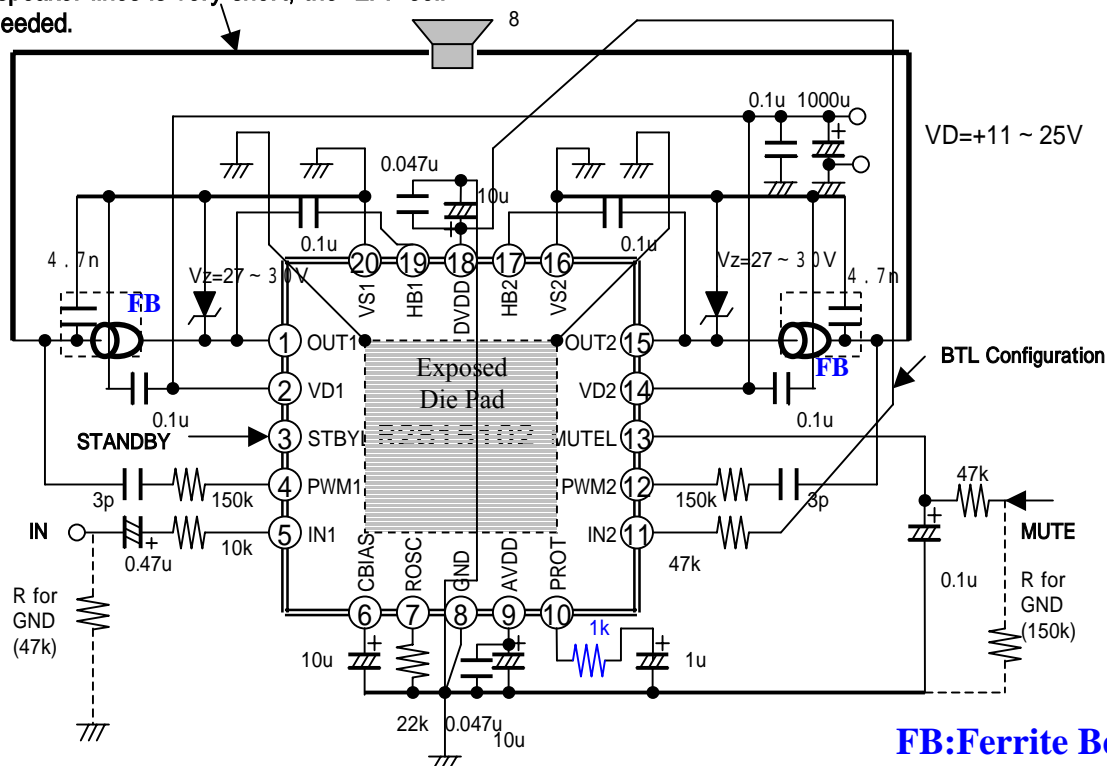


Fig.7 BTL operation mode without output LPF coil

If this speaker lines is very short, the LPF coil
is not needed.



24-bit, 192kHz Stereo Codec with 5 Channel I/P Multiplexer

DESCRIPTION

The WM8776 is a high performance, stereo audio codec with five channel input selector. The WM8776 is ideal for surround sound processing applications for home hi-fi, DVD-RW and other audio visual equipment.

A stereo 24-bit multi-bit sigma delta ADC is used with a five stereo channel input mixer. Each ADC channel has programmable gain control with automatic level control. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHz to 96kHz are supported.

A stereo 24-bit multi-bit sigma delta DAC is used with digital audio input word lengths from 16-32 bits and sampling rates from 32kHz to 192kHz. The DAC has an input mixer allowing an external analogue signal to be mixed with the DAC signal. There are also Headphone and line outputs, with volume controls for the headphones.

The WM8776 supports fully independent sample rates for the ADC and DAC. The audio data interface supports I²S, left justified, right justified and DSP formats.

The device is controlled in software via a 2 or 3 wire serial interface, selected by the MODE pin, which provides access to all features including channel selection, volume controls, mutes, and de-emphasis facilities.

The device is available in a 48-pin TQFP package.

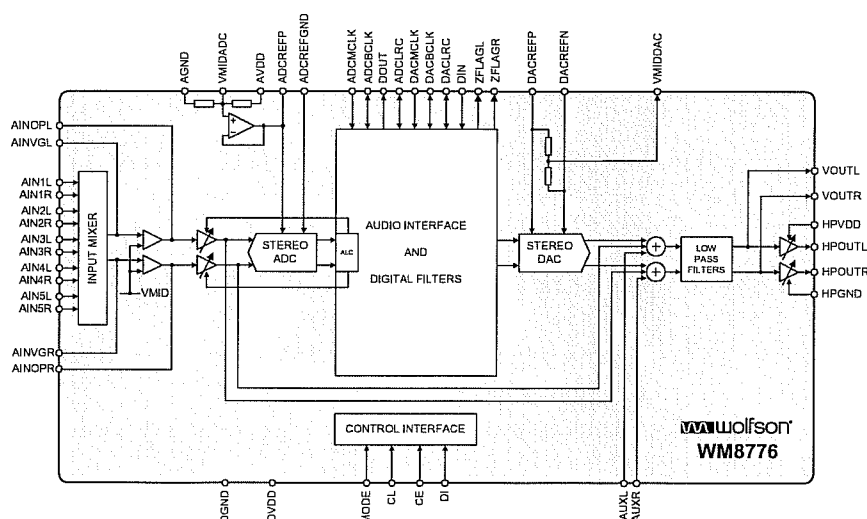
FEATURES

- Audio Performance
 - 108dB SNR ('A' weighted @ 48kHz) DAC
 - 102dB SNR ('A' weighted @ 48kHz) ADC
- DAC Sampling Frequency: 32kHz – 192kHz
- ADC Sampling Frequency: 32kHz – 96kHz
- Five stereo ADC inputs with analogue gain adjust from +24dB to –21dB in 0.5dB steps
- Programmable Limiter or Automatic Level Control (ALC)
- Stereo DAC with independent analogue and digital volume controls
- Stereo Headphone and Line Output
- 3-Wire SPI Compatible or 2-Wire Software Serial Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
 - I²S, Left, Right Justified or DSP
 - 16/20/24/32 bit Word Lengths
- Analogue Bypass Path Feature
- Selectable AUX input to the volume controls
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation

APPLICATIONS

- Surround Sound AV Processors and Hi-Fi systems
- DVD-RW

BLOCK DIAGRAM



Pin diagram of the AD7792-1. The diagram shows a 48-pin package with pins numbered 1 to 48. Pins 1-12 are on the left, 13-24 on the bottom, 25-36 on the right, and 37-48 on the top. A black dot is located at pin 47. The pin functions are:

- 1 AIN2L
- 2 AIN1R
- 3 AIN1L
- 4 DACBCLK
- 5 DACMCLK
- 6 DIN
- 7 DACLRC
- 8 ZFLAGR
- 9 ZFLAGL
- 10 ADCBCLK
- 11 ADCMCLK
- 12 DOUT
- 13 ADCLRC
- 14 DGND
- 15 DVDD
- 16 MODE
- 17 CE
- 18 DI
- 19 CL
- 20 HPFOUTL
- 21 HPFND
- 22 HPVDD
- 23 HPFOUTR
- 24 NC
- 25 VOUTL
- 26 VOUTR
- 27 VMIDDAC
- 28 DACREFN
- 29 DACREFP
- 30 AUXR
- 31 AUXL
- 32 VMIDADC
- 33 ADCREFGND
- 34 ADCREFP
- 35 AVDD
- 36 AVDD
- 37 AIN0GR
- 38 AIN0GL
- 39 AIN0PR
- 40 AIN0PL
- 41 AIN6L
- 42 AIN6R
- 43 AIN4L
- 44 AIN4R
- 45 AIN3L
- 46 AIN3R
- 47 AIN3L
- 48 AIN2R

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8776EFT/V	-25 to +85°C	48-pin TQFP	MSL2	240°C
WM8776EFT/RV	-25 to +85°C	48-pin TQFP (tape and reel)	MSL2	240°C
WM8776SEFT/V	-25 to +85°C	48-pin TQFP (lead free)	MSL2	260°C
WM8776SEFT/RV	-25 to +85°C	48-pin TQFP (lead free, tape and reel)	MSL2	260°C

Reel quantity = 2,200

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AIN2L	Analogue Input	Channel 2 left input multiplexor virtual ground
2	AIN1R	Analogue Input	Channel 1 right input multiplexor virtual ground
3	AIN1L	Analogue Input	Channel 1 left input multiplexor virtual ground
4	DACBCLK	Digital input/output	DAC audio interface bit clock
5	DACMCLK	Digital input	Master DAC clock; 256, 384, 512 or 768fs (fs = word clock frequency)
6	DIN	Digital Input	DAC data input
7	DACLRC	Digital input/output	DAC left/right word clock
8	ZFLAGR	Open Drain output	DAC Right Zero Flag output (external pull-up resistor required)
9	ZFLAGL	Open Drain output	DAC Left Zero Flag output (external pull-up resistor required)
10	ADCBCLK	Digital input/output	ADC audio interface bit clock
11	ADCMCLK	Digital input	ADC audio interface master clock
12	DOUT	Digital output	ADC data output
13	ADCLRC	Digital input/output	ADC left/right word clock
14	DGND	Supply	Digital negative supply
15	DVDD	Supply	Digital positive supply
16	MODE	Digital input	Control interface mode select (5V tolerant)
17	CE	Digital input	Serial interface Latch signal (5V tolerant)
18	DI	Digital input	Serial interface data (5V tolerant)
19	CL	Digital input	Serial interface clock (5V tolerant)
20	HPOUTL	Analogue Output	Headphone left channel output
21	HPGND	Supply	Headphone negative supply
22	HPVDD	Supply	Headphone positive supply
23	HPOUTR	Analogue Output	Headphone right channel output
24	NC	Not bonded	
25	NC	Not bonded	
26	VOUTL	Analogue output	DAC channel left output
27	VOUTR	Analogue output	DAC channel right output
28	VMIDDAC	Analogue output	DAC midrail decoupling pin ; 10uF external decoupling
29	DACREFN	Analogue input	DAC negative reference input
30	DACREFP	Analogue input	DAC positive reference input
31	AUXR	Analogue input	DAC mixer right channel input
32	AUXL	Analogue input	DAC mixer left channel input
33	VMIDADC	Analogue Output	ADC midrail divider decoupling pin; 10uF external decoupling
34	ADCREFGND	Supply	ADC negative supply and substrate connection
35	ADCREFP	Analogue Output	ADC positive reference decoupling pin; 10uF external decoupling
36	AVDD	Supply	Analogue positive supply
37	AGND	Supply	Analogue negative supply and subVstrate connection
38	AINVGR	Analogue Input	Right channel multiplexor virtual ground
39	AINOPR	Analogue Output	Right channel multiplexor output
40	AINVGL	Analogue Input	Left channel multiplexor virtual ground
41	AINOPL	Analogue Output	Left channel multiplexor output
42	AIN5R	Analogue Input	Channel 5 right input multiplexor virtual ground
43	AIN5L	Analogue Input	Channel 5 left input multiplexor virtual ground
44	AIN4R	Analogue Input	Channel 4 right input multiplexor virtual ground
45	AIN4L	Analogue Input	Channel 4 left input multiplexor virtual ground
46	AIN3R	Analogue Input	Channel 3 right input multiplexor virtual ground
47	AIN3L	Analogue Input	Channel 3 left input multiplexor virtual ground
48	AIN2R	Analogue Input	Channel 2 right input multiplexor virtual ground

Note : Digital input pins have Schmitt trigger input buffers and pins 16, 17, 18 and 19 are 5V tolerant.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs (DI, CL, CE and MODE)	DGND -0.3V	+7V
Voltage range digital inputs (MCLK, DIN, ADCLRC, DACLRC, ADCBCLK and DACBCLK)	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T _A	-25°C	+85°C
Storage temperature	-65°C	+150°C

Notes:

- Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD, HPVDD, DACREFP		2.7		5.5	V
Ground	AGND, DGND, DACREFN, ADCREFGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V

Note: digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, f_s = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V _{IL}				0.8	V
Input HIGH level	V _{IH}		2.0			V
Output LOW	V _{OL}	I _{OL} =1mA			0.1 x DVDD	V
Output HIGH	V _{OH}	I _{OH} =1mA	0.9 x DVDD			V
Analogue Reference Levels						
Reference voltage	V _{VMID}			AVDD/2		V
Potential divider resistance	R _{VMID}			50k		Ω
DAC Performance (Load = 10k Ω, 50pF)						
0dBFs Full scale output voltage				1.0 x AVDD/5		Vrms
SNR (Note 1,2)		A-weighted, @ fs = 48kHz		108		dB
SNR (Note 1,2)		A-weighted @ fs = 96kHz		108		dB
Dynamic Range (Note 2)	DNR	A-weighted, -60dB full scale input		108		dB
Total Harmonic Distortion (THD)		1kHz, 0dBFs		-97	-90	dB
DAC channel separation				100		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Headphone Buffer						
Maximum Output voltage				0.9		Vrms
Max Output Power (Note 4)	P _o	R _L = 32 Ω		25		mW
		R _L = 16 Ω		50		mW
SNR (Note 1,2)		A-weighted	85	92		dB
Headphone analogue Volume Gain Step Size			0.5	1	1.5	dB
Headphone analogue Volume Gain Range		1kHz Input	-73		+6	dB
Headphone analogue Volume Mute Attenuation		1kHz Input, 0dB gain		100		dB
Total Harmonic Distortion +Noise	THD+N	1kHz, R _L = 32Ω @ P _o = 10mW rms		-80 0.01	-60 0.1	dB %
		1kHz, R _L = 32Ω @ P _o = 20mW rms		-77 0.014	-40 1.0	dB %
Power Supply Rejection Ratio	PSRR	20Hz to 20kHz, without supply decoupling		-40		dB
ADC Performance						
Input Signal Level (0dB)				1.0 x AVDD/5		Vrms
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 48kHz		102		dB
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 96kHz 64 x OSR		100		dB
Dynamic Range (note 2)		A-weighted, -60dB full scale input		102		dB
Total Harmonic Distortion (THD)		1kHz, 0dBFs		-90	-80	DB

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, f_s = 48kHz, MCLK = 256fs unless otherwise stated.

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, I _A = 20 mA, f _s = 40kHz, MCLK = 200Hz unless otherwise stated.						
ADC Channel Separation		1kHz, -3dBFS		-95	-85	dB
Programmable Gain Step Size		1kHz Input		90		dB
Programmable Gain Range (Analogue)		1kHz Input	-21	0.5	0.75	dB
Programmable Gain Range (Digital)		1kHz Input	-103		-21.5	dB
Mute Attenuation (Note 6)		1kHz Input, 0dB gain		76		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Analogue input (AIN) to Analogue output (VOUT) (Load=10k Ω, 50pF, gain = 0dB) Bypass Mode						
0dB Full scale output voltage				1.0 x AVDD/5		Vrms
SNR (Note 1)			90	100		dB
THD		1kHz, 0dB		-90		dB
		1kHz, -3dB		-95		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Mute Attenuation		1kHz, 0dB		100		dB
Supply Current						
Analogue supply current		AVDD = 5V		48		mA
Digital supply current		DVDD = 3.3V		8		mA

Notes:

- Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
- All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
- VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
- Harmonic distortion on the headphone output decreases with output power.
- All performance measurement done using certain timings conditions (Please refer to section 'Digital Audio Interface').
- A better MUTE Attenuation can be achieved if the ADC gain is set to minimum.

TERMINOLOGY

- Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
- Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
- THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
- Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
- Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
- Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

CPT TFT-LCD

CLAA320WA01 C

ACCEPTED BY :

APPROVED BY	CHECKED BY	PREPARED BY

RECORD OF REVISIONS

Revision No.	Date	Page	Description
Ver1.0	2005/8/29	all	Preliminary specification was first issued.
Ver2.0	2005/9/28	3	Module Weight = 8000(Max)→8200(Max)
		4	Input Voltage of Inverter =21.6 (Min)→ -0.3(Min) Input Voltage of Inverter =26.4 (Max)→27 (Max) Inverter Dimming=0 (Min)→ -0.3(Min) Inverter Dimming=5(Max)→5.5(Max) Backlight on Control Voltage=2(Min)→ -0.3(Min) Backlight on Control Voltage=5(Max)→5.5(Max)
		5	LCD Power Supply Current—White=400(Typ.)→350(Typ.) LCD Power Supply Current—White= -- (Max)→400(Max) LCD Power Supply Current—Black=350(Typ.)→300(Typ.) LCD Power Supply Current—Black= --(Max)→400(Max) LCD Power Supply Current—RGB stripe=390(Typ.)→320(Typ.) LCD Power Supply Current—RGB stripe= --(Max)→400(Max)
		8	Input Frequency of Inverter=60.5(Min)→61.5(Min) Input Frequency of Inverter=66.5(Max)→65.5(Max)
		10	Pin 25=NC→DE/Sync
		13	DCLK Freq.=68(Min)→62(Min) Horizontal Line Rate=43.2(Min)→37.1(Min) Horizontal Line Rate=48.5(Typ.)→48.6(Typ.) Horizontal Line Rate=53.3(Max)→56Max Horizontal Effective Time= --(Min)→1366(Min) Horizontal Effective Time= --(Max)→1366(Max) Vertical Frame Rate=54.6(Min)→47(Min) Vertical Frame Rate=67.5(Max)→63(Max)
		22	Response Time Tr= 9(Typ.)→10(Typ.) Response Time Tr=16(Max)→17(Max) Response Time Tf= 7(Typ.)→6(Typ.) Response Time Tf=9(Max)→8(Max)
	2005/10/13	3	Module Weight = 8200(Max)→8300(Max)
		8	Power Consumption=(115, Typ)→(120, Typ)

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1. OVERVIEW

CLAA320WA01 is 32" color (80.04cm) TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, LVDS driver ICs, control circuit, backlight, and inverter. By applying 8 bit digital data, 1366*768, 16.7 million-color images are displayed on the 32" diagonal screen. General specification are summarized in the following table:

1.1 GENERAL INFORMATION

ITEM		SPECIFICATION
Display Area (mm)		697.68 (H) × 392.25 (V) (31.51 inch diagonal)
Number of Pixels		1366 (H) × 768 (V) 16:9
Pixel Pitch (mm)		0.51075 (H) × 0.51075 (V)
Color Pixel Arrangement		RGB Vertical Strip
Display Mode		Normally Black
Number of Colors		16.7M (8bit)
Surface Treatment		Hard coating: 2H Anti-Clare + LR <less than 2% reflection.
Wide view tech.		MVA
Viewing Angle	CR ≥ 10	-85~85(H), --85~85(V)
Brightness (cd/m2)		550 (Typ.)
Total Module Power (W)		125
Module Size (mm)		743.0±1(W) × 447.0±1 (H) × 44.0±1 (D) (including inverter)
Module Weight (g)		8300 (Max)

1.2 MECHANICAL INFORMATION

ITEM			MIN	TYP.	MAX.	UNIT
Module outline dimension	Horizontal (H)		742.0	743.0	744.0	mm
	Vertical (V)		446.0	447.0	448.0	mm
	Depth (D)	with inverter	43.0	44.0	45.0	mm
Module Weight			--	--	8300	g

2. ABSOLUTE MAXIMUM RATINGS

The following are maximum values which, if exceeded, may cause faulty operation or damage to the module.

ITEM	SYMBOL	MIN.	MAX.	UNIT	REMARK
Power Supply Voltage For LCD	VCC	- 0.3	15.0	V	
Input voltage of inverter	VBL	- 0.3	27	V	
Inverter dimming	VDIM	- 0.3	5.5	Vdc	
Backlight on control voltage	VBLON	- 0.3	5.5	Vdc	
ESD	VESDt	-100	100	V	
	VESDc	-8000	8000	V	
Operation Ambient Temperature	T _{op}	0	50	°C	*1) *2) *3) *4)
Storage Temperature	T _{stg}	-20	60	°C	*1) *2) *3) *4)

[Note]

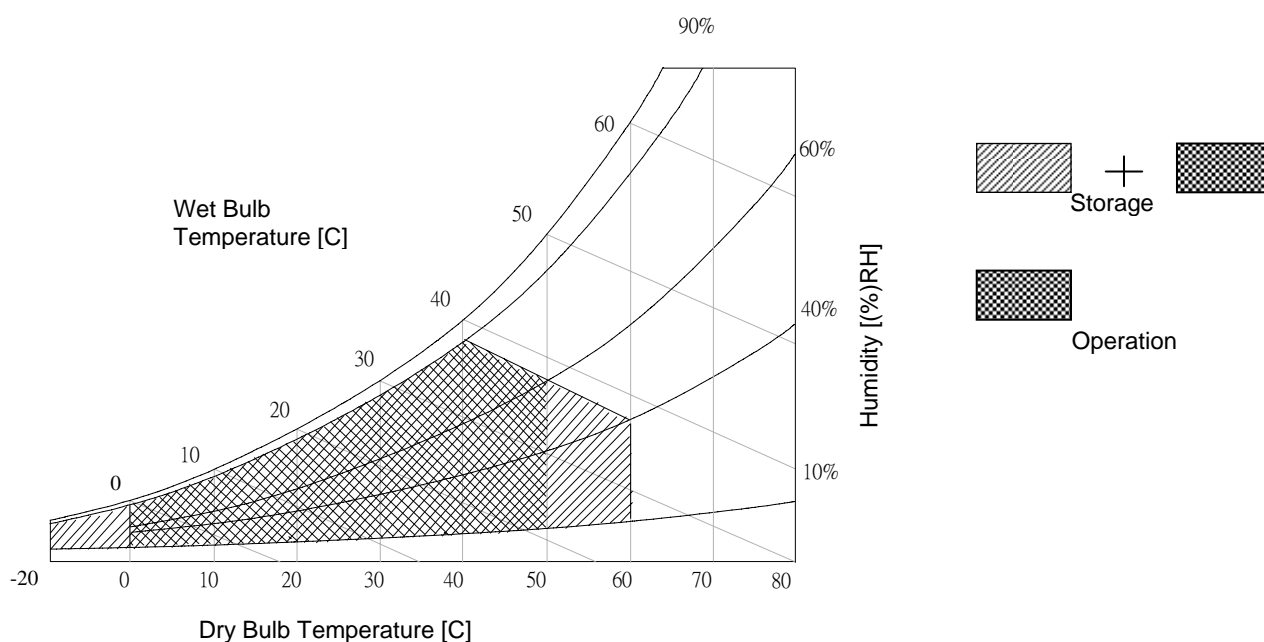
- *1) The relative temperature and humidity range are as below sketch. (90%RHMax / Ta ≤ 40°C)
- *2) The maximum wet bulb temperature ≤ 39°C (Ta > 40°C) and without dewing.
- *3) If you use the product in a environment which over the definition of temperature and humidity too long, and it will effect the result of visible inspection.
- *4) While the product operates in normal temperature range, the center surface of panel should be under 60°C.
- *5) Input voltage of the connector side in Inverter.

Humidity:

Humidity ≤ 85%RH without condensation.

Relative Humidity ≤ 90% (Ta ≤ 40°C)

Wet Bulb Temperature ≤ 39°C (Ta ≥ 40°C)



3. ELECTRICAL CHARACTERISTICS

3.1 TFT-LCD MODULE

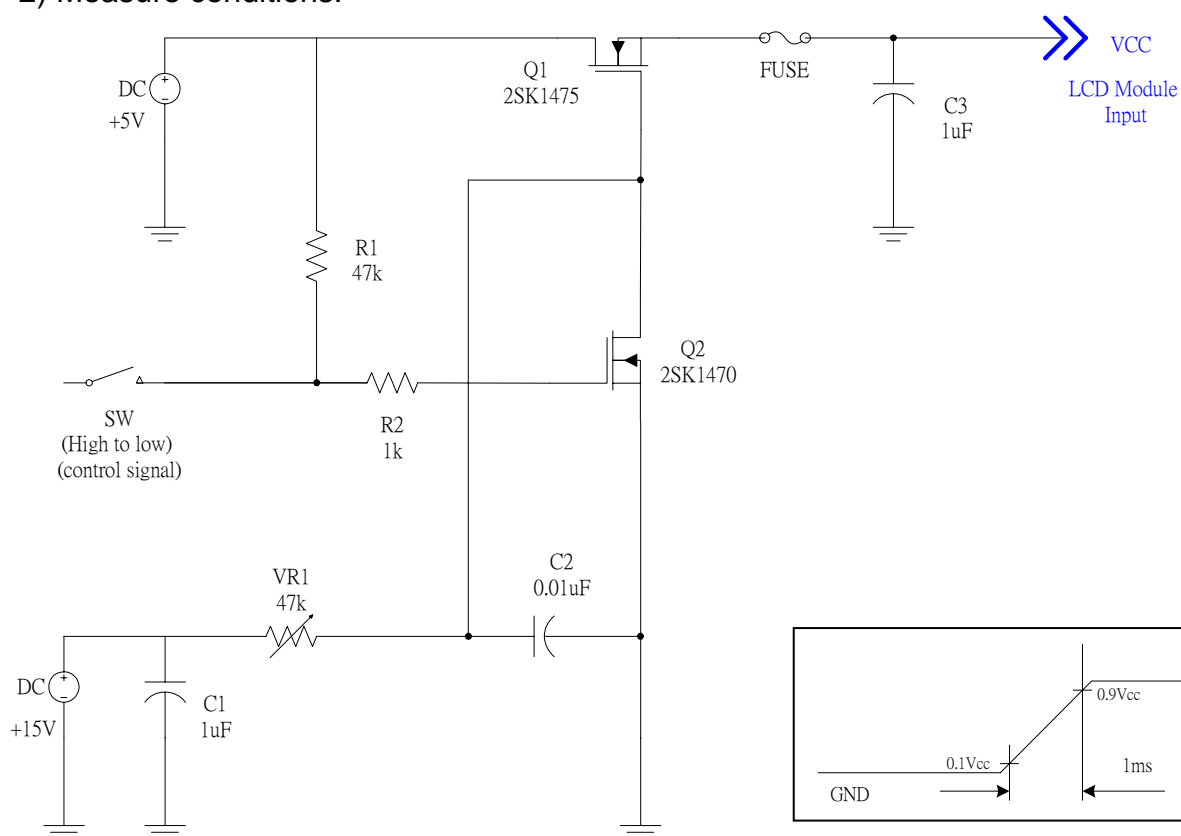
Ta=25°C

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
LCD Power Supply Voltage		VCC	11.4	12.0	12.6	V	*1)
Ripple Voltage		Vrpd	--	--	100	mVp-p	VIN=+12.0V
Rush current		Irush	--	--	8	A	*2)
LCD Power Supply Current	White	ICC	--	350	400	mA	*3)
	Black		--	300	400		
	RGB stripe		--	320	400		
LCD power consumption		Pc	--	6.48	9.7	W	
High input voltage of LVDS		V _{IN+}	--	--	100	mV	*4) *5)
Low input voltage of LVDS		V _{IN-}	100	--	--	mV	
Input common voltage of LVDS		VCM	--	1.25	-	V	
Input terminal resist of LVDS		R _T	--	100	--	ohm	

[Note]

*1) The module should be always operated within above ranges.

*2) Measure conditions:



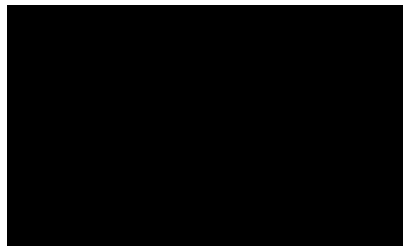
Vcc rising time is 1 ms

*3) The specified power supply current is under condition at $V_{CC}=12V$, $T_a=25\pm 2^{\circ}C$, $f_v=60Hz$, whereas a power dissipation check pattern below is displayed.

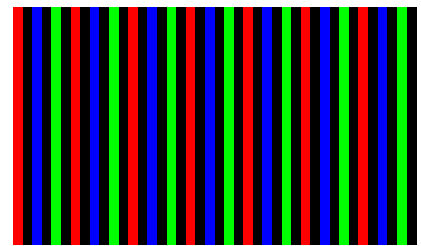
a. White pattern



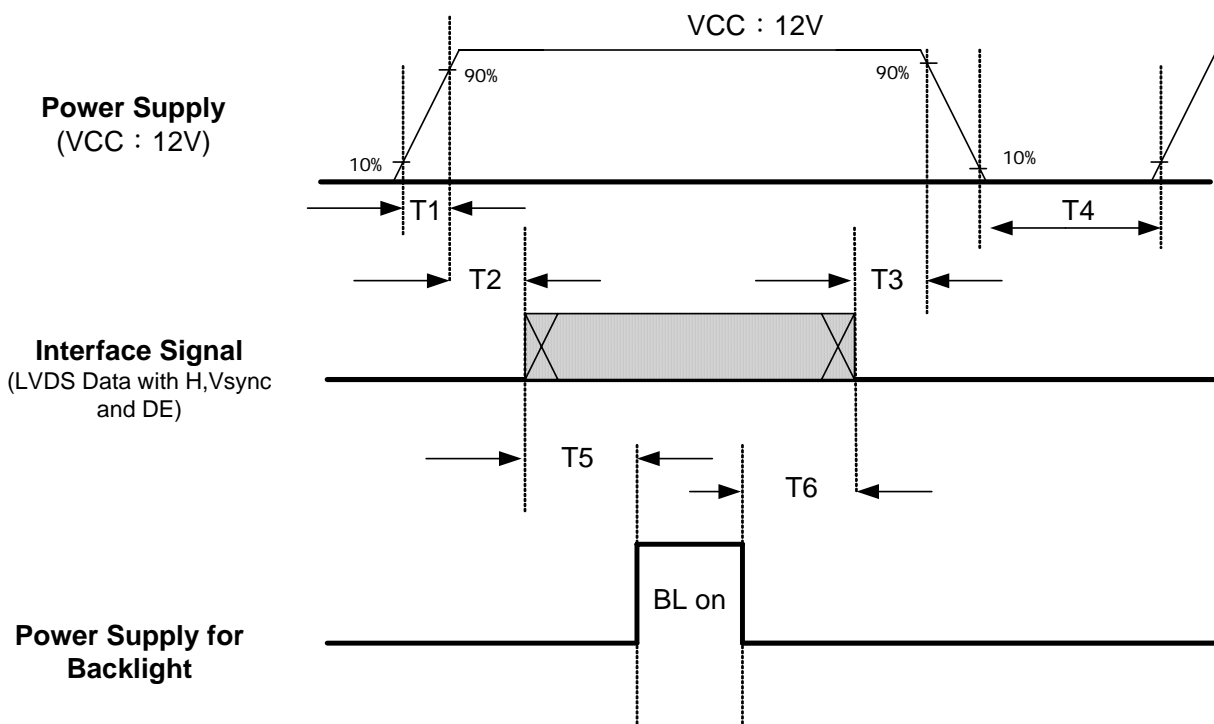
b. Black pattern



c. RGB Stripe pattern



*4) Power and Signal Sequence:



Power Sequence Table

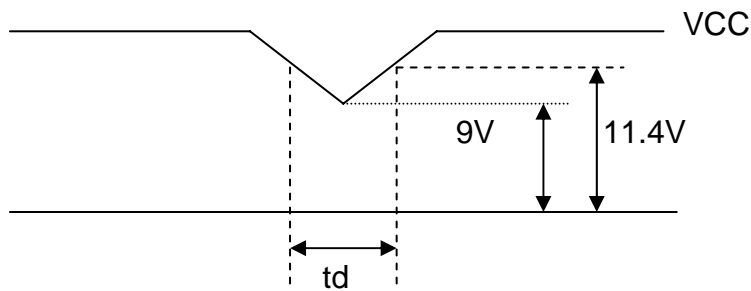
Parameter	Value			Unit
	Min	Typ	Max	
T1	1	---	30	ms
T2	0	---	50	ms
T3	0	---	50	ms
T4	2000	---		ms
T5	110	---		ms
T6	100	---		ms

Notes:

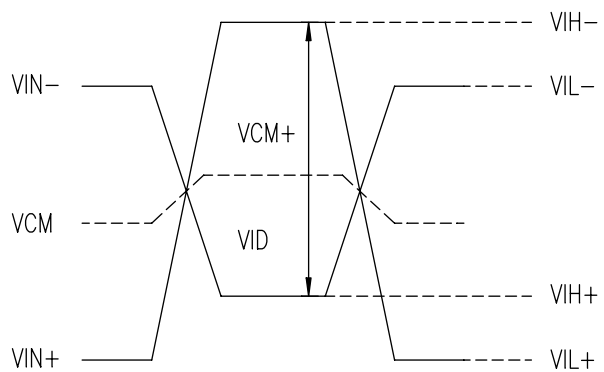
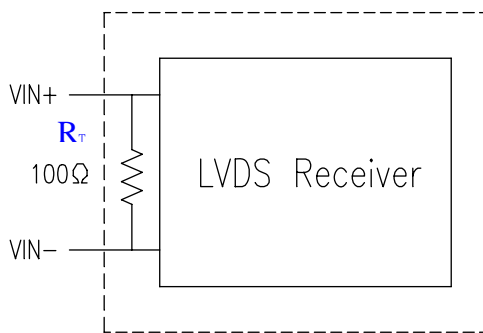
- Please avoid floating state of interface signal at invalid period.
- When the interface signal is invalid, be sure to pull down the power supply for LCD to 0V.
- Lamp power must be turn off after power supply for LCD interface signal valid.

VCC-dip State:

- 1) When $9V \leq VCC < 11.4V$, $t_d \leq 10$ ms.
- 2) $VCC > 11.4V$, VCC-dip condition should also follow the VCC-turn-off condition.



*5) LVDS Signal Definition:



$$VID = VIN_+ - VIN_-$$

$$\Delta VCM = |VCM_+ - VCM_-|$$

$$\Delta VID = |VID_+ - VID_-|$$

$$VID_+ = |VIH_+ - VIH_-|$$

$$VID_- = |VIL_+ - VIL_-|$$

$$VCM = (VIN_+ + VIN_-) / 2$$

$$VCM_+ = (VIH_+ + VIH_-) / 2$$

$$VCM_- = (VIL_+ + VIL_-) / 2$$

VIN+: Positive Polarity differential DATA & CLK input

VIN-: Negative Polarity differential DATA & CLK input

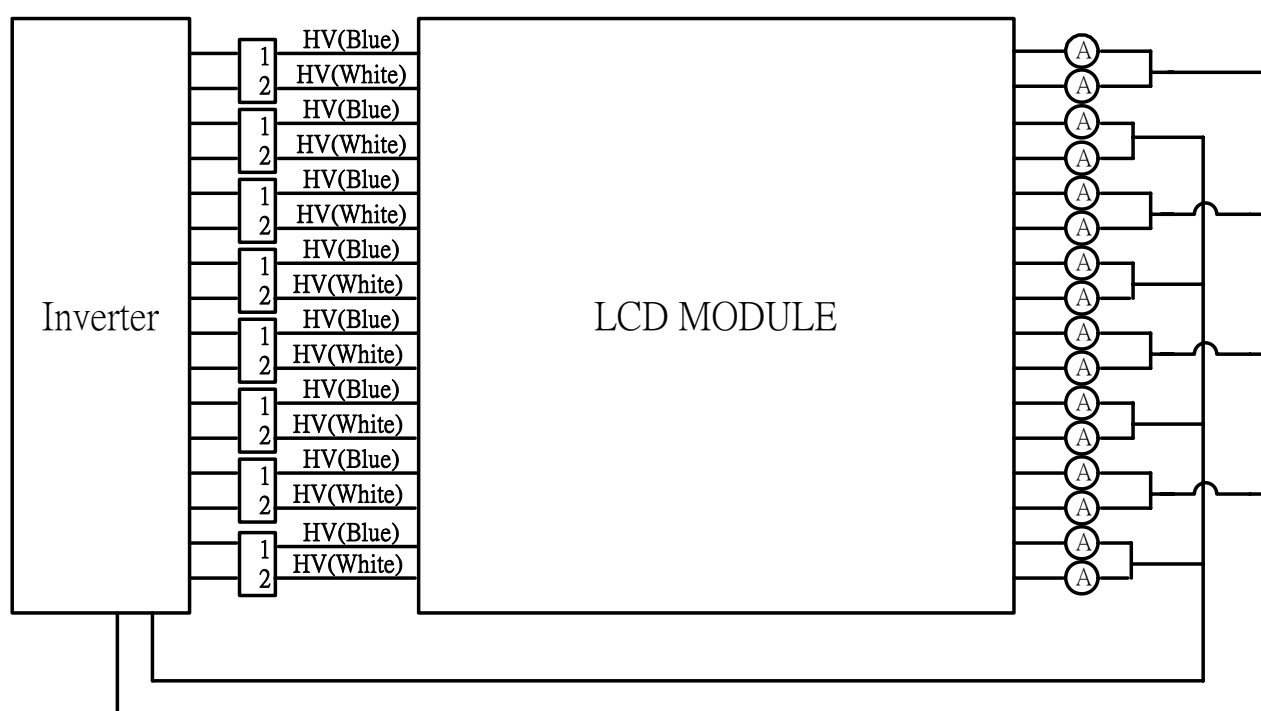
3.2 BACKLIGHT

Ta=25℃

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	REMARK
Lamp Voltage	VL	--	1150	--	Vrms	IL=5.0mA
Lamp Current	IL	4.0	4.5	5.0	mA _{rms}	*1)
Lamp life time	LT	50,000	--	--	hr	*2)
Input voltage of inverter	VBL	21.6	24	26.4	V	*3)
Input current of inverter	IIN ⁰	--	(4.8)	--	A	*4)
	IIN		(4.4)			*5)
Input frequency of inverter	FL	61.5	63.5	65.5	KHz	*6)
Inverter dimming	VDIM	0	--	5	V _{dc}	*7)
Inverter duty ratio	--	20	--	100	%	VDIM=5V(MAX.)
Inverter opening voltage	Vopen	1900	--	--	Vrms	
Backlight on /of control voltage	ON	V _{B_{BLON}}	2.0	--	V	
	OFF		0	--		
Power consumption (Panel+ Backlight)	BLW ⁰	--	(120)	--	W	*4)
	BLW	--	(105)	--		*5)

[Note]

- *1) Lamp Current measurement method (The current meter is connected to low voltage end)
Take the average of 16 CCFL's lamp current as V_{DIM} = 5V after power on for 30 min.



*2) Definition of the lamp life time:

When lamp luminance reduce to 50% or lower than its initial value.

*3) Ripple voltage that occur at the instant of power-on can't exceed 30V.

*4) 25°C; $V_{DIM} = 5V(MAX.)$, After power on for 5 seconds

*5) 25°C; $V_{DIM} = 5V(MAX.)$, After power on for 30 minutes

*6) Electrical and optical characteristics color chromaticity is not included can maintain in a range +/- 10% when the inverter operates within this frequency range.

*7) Brightness is the darkest when $V_{DIM} = 0V$;

Brightness is the brightest when $V_{DIM} = 5V$.

4. INTERFACE PIN CONNECTION

4.1 Connector Part No.: 20389-030E(I-PEX), FI-X30SSL-HF(JAE), or compatible

Pin NO	Symbol	Description	Note
1	VCC	Power supply: +12V	
2	VCC	Power supply: +12V	
3	GND	Ground	
4	GND	Ground	
5	RxIN0-	Data-	
6	RxIN0+	Data+	
7	GND	Ground	
8	RxIN1-	Data-	
9	RxIN1+	Data+	
10	GND	Ground	
11	RxIN2-	Data-	
12	RxIN2+	Data+	
13	GND	Ground	
14	RxCLKIN-	Clock-	
15	RxCLKIN+	Clock+	
16	GND	Ground	
17	RxIN3-	Data-	
18	RxIN3+	Data+	
19	GND	Ground	
20	NC	Reserved	*1)
21	NC	Reserved	*1)
22	NC	Reserved	*1)
23	NC	Reserved	*1)
24	NC	Reserved	*1)
25	DE/Sync	DE/Sync Option	*3)
26	NC	Reserved	*1)
27	DMS	LVDS Option	*2)
28	NC	Reserved	*1)
29	NC	Reserved	*1)
30	GND	Ground	

*1) NC: Must let it open.

*2) LVDS OPTION PIN (DMS):

DMS (Pin 27)	LVDS format
GND	Non-JEIDA
NC	JEIDA

*3) DE / Sync:

DE/Syncs (Pin 25)	Mode
NC	DE
GND	Sync

4.2 LVDS INTERFACE:

LVDS RECEIVER: Tcon (LVDS Rx merged)

	LVDS Pin	JEIDA-DATA	Non-JEIDA-DATA
TxOUT/RxIN0	TxIN/RxOUT0	R2	R0
	TxIN/RxOUT1	R3	R1
	TxIN/RxOUT2	R4	R2
	TxIN/RxOUT3	R5	R3
	TxIN/RxOUT4	R6	R4
	TxIN/RxOUT6	R7	R5
	TxIN/RxOUT7	G2	G0
TxOUT/RxIN1	TxIN/RxOUT8	G3	G1
	TxIN/RxOUT9	G4	G2
	TxIN/RxOUT12	G5	G3
	TxIN/RxOUT13	G6	G4
	TxIN/RxOUT14	G7	G5
	TxIN/RxOUT15	B2	B0
	TxIN/RxOUT18	B3	B1
TxOUT/RxIN2	TxIN/RxOUT19	B4	B2
	TxIN/RxOUT20	B5	B3
	TxIN/RxOUT21	B6	B4
	TxIN/RxOUT22	B7	B5
	TxIN/RxOUT24	Hsync	Hsync
	TxIN/RxOUT25	Vsync	Vsync
	TxIN/RxOUT26	DENA	DENA
TxOUT/RxIN3	TxIN/RxOUT27	R0	R6
	TxIN/RxOUT5	R1	R7
	TxIN/RxOUT10	G0	G6
	TxIN/RxOUT11	G1	G7
	TxIN/RxOUT16	B0	B6
	TxIN/RxOUT17	B1	B7
	TxIN/RxOUT23	Reserved	Reserved

4.3 INVERTER – CONNECTOR:

Connector (Receptacle): S14B-PH-SM3-TB (JST) or compatible

Mating connector (Plug): PRH-14(JST) or compatible

Pin No.	Symbol	Description	Note
1	VBL	Supply Voltage 24V	
2	VBL	Supply Voltage 24V	
3	VBL	Supply Voltage 24V	
4	VBL	Supply Voltage 24V	
5	VBL	Supply Voltage 24V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	NC	NC (Test pin or else)	
12	BLON	ON/OFF Control	(1)
13	VDIM	0V~5V	(2)
14	GND	GND	

[Note]

*1) ON/ OFF control: ON=5V, OFF=0V; when this PIN is disconnecting with power, the Inverter is in OFF status.

*2) VDIM: MAX=5V, MIN=0V; when this PIN is disconnecting with power, the output status of Inverter is the same as VDIM=0.

5. INTERFACE TIMING (DE only mode)

5.1 TIMING SPECIFICATION

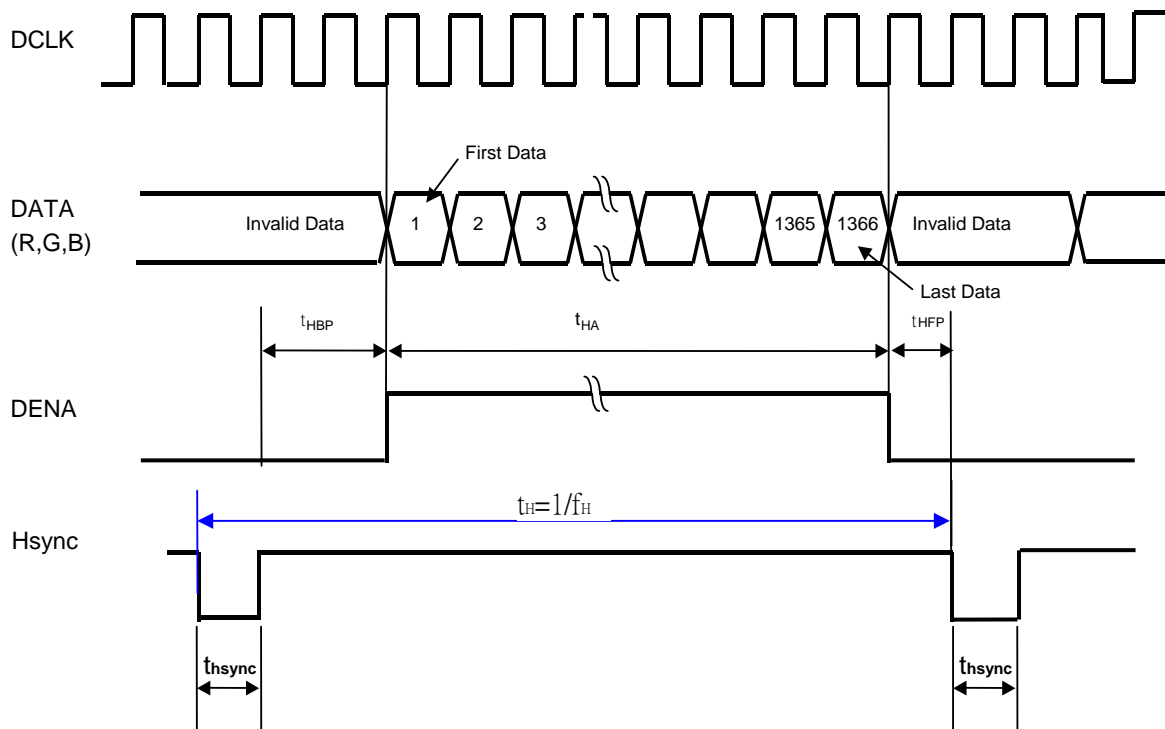
ITEM			SYMBOL	MIN.	TYP.	MAX.	UNIT	
LCD Timing	DCLK		Freq.	f _{CLK}	62	80	84	MHz
			Cycle	t _{CLK}	14.7	12.5	11.9	ns
	DENA	Horizontal	Line Rate	f _H	37.1	48.6	56	kHz
			Horizontal Total Time	t _H	1575	1648	1936	t _{CLK}
			Horiaontal Effective Time	t _{HA}	1366	1366	1366	t _{CLK}
			Horizontal Blank Time	t _{HB}	209	282	570	t _{CLK}
		Vertical	Frame Rate	Fr	47	60	63	Hz
			Vertical Total Time	t _V	790	810	888	t _H
			Vertical Effective Time	t _{VA}	768	768	768	t _H
			Vertical Blank Time	t _{VB}	22	42	120	t _H
	Sync Mode	Horizontal	Horizontal sync time	t _{Hsync}	---	136	---	t _{CLK}
			Horizontal Back porch	t _{HBP}	---	108	---	t _{CLK}
		Vertical	Vertical sync time	t _{Vsync}	---	5	---	t _H
			Vertical Back porch	t _{VBP}	---	22	---	t _H

[Note]

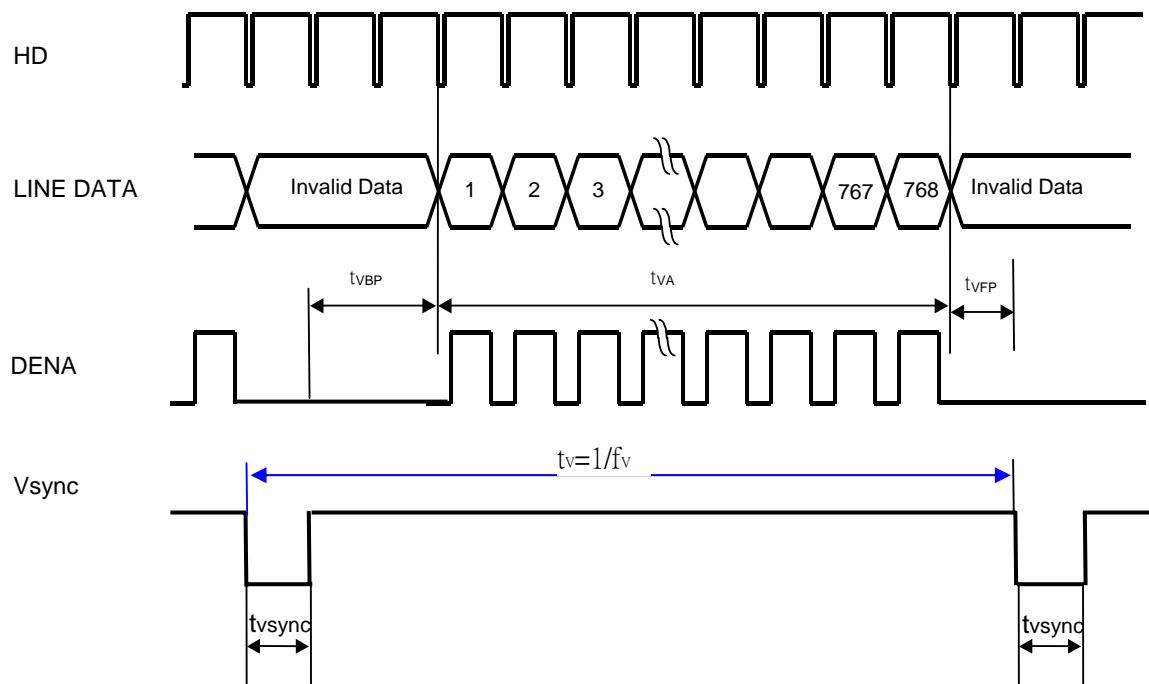
1).The best result of over-driving is in frame rate =60Hz.

5.2 TIMING CHART

a. Horizontal Timing

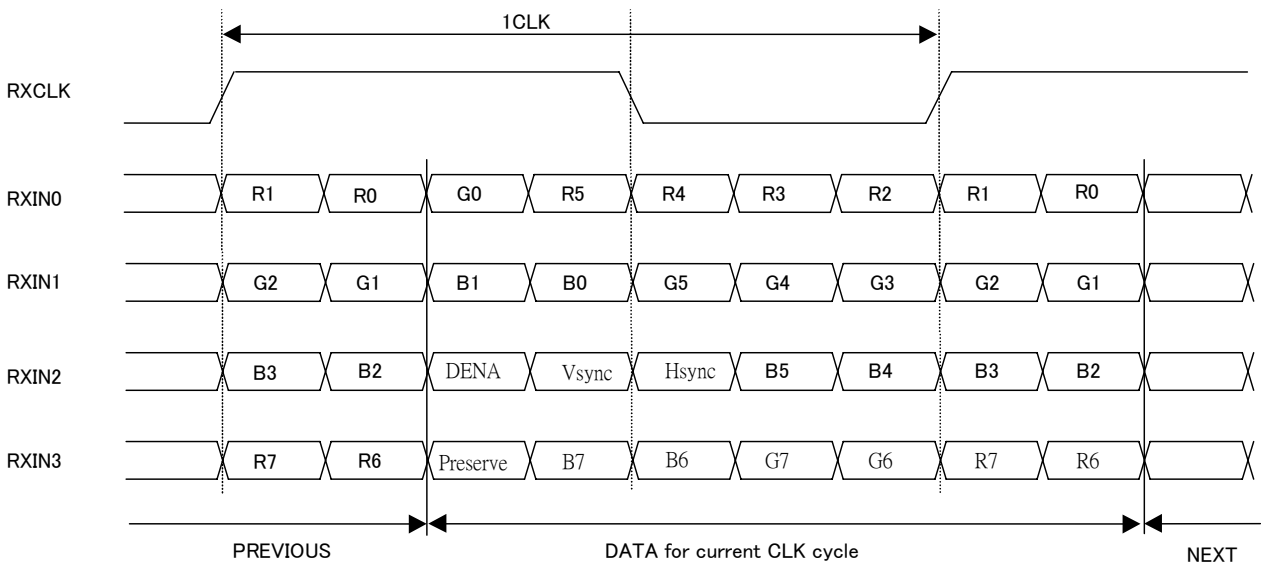


b. Vertical Timing Chart

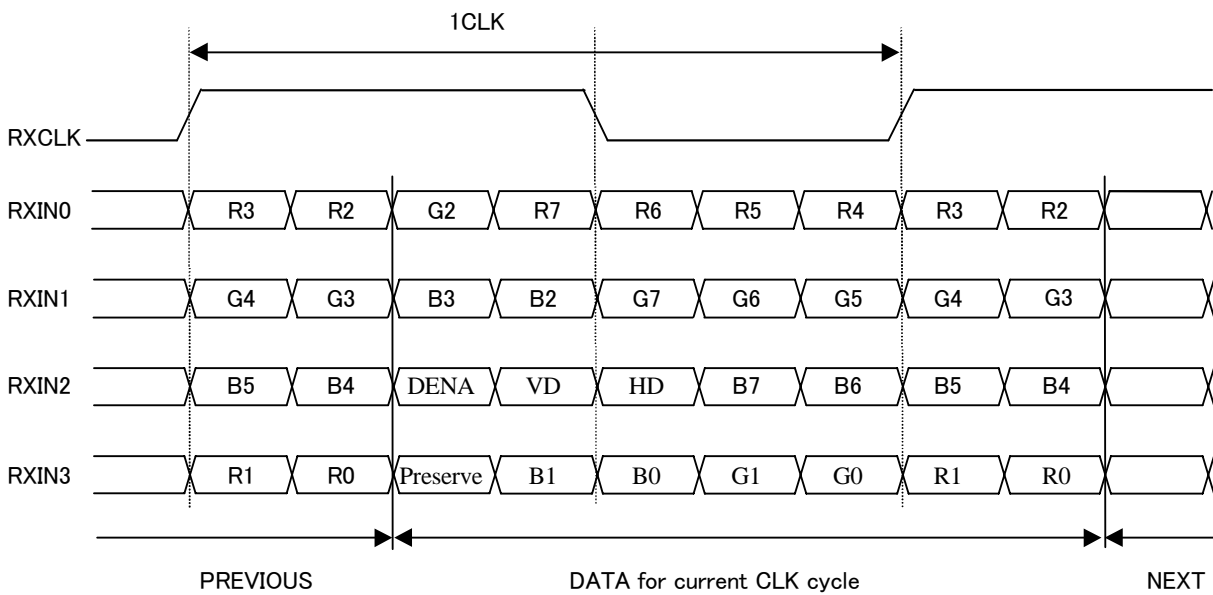


5.3 LVDS DATA MAPPING

a. None-JEIDA normal Specification



b. JEIDA Specification



8bit LSB: R0,G0,B0

Parallel TTL Data Inputs Mapped to LVDS outputs

5.4 LVDS INTERFACE

8bit LSB: R0, G0, B0

JEIDA: Parallel TTL Data Inputs Mapped to LVDS outputs

TRANSMITTER(THC63LVD823)		INTERFACE CONNECTOR		TIMING CONTROLLER INPUT
PIN NO	INPUT DATA	HOST	TFT_LCD	
51	TA0	TxOUT0+ TxOUT0-	TA+ TA-	R2
52	TA1			R3
54	TA2			R4
55	TA3			R5
56	TA4			R6
3	TA5			R7 (MSB)
4	TA6			G2
6	TB0	TxOUT1+ TxOUT1-	TB+ TB-	G3
7	TB1			G4
11	TB2			G5
12	TB3			G6
14	TB4			G7 (MSB)
15	TB5			B2
19	TB6			B3
20	TC0	TxOUT2+ TxOUT2-	TC+ TC-	B4
22	TC1			B5
23	TC2			B6
24	TC3			B7 (MSB)
27	TC4			Hsync
28	TC5			Vsync
30	TC6			DENA
50	TD0	TxOUT3+ TxOUT3-	TD+ TD-	R0 (LSB)
2	TD1			R1
8	TD2			G0 (LSB)
10	TD3			G1
16	TD4			B0 (LSB)
18	TD5			B1
25	TD6			Reserved

5.5 COLOR DATA ASSIGNMENT

COLOR	INPUT DATA	B DATA								G DATA								R DATA							
		B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0
		MSB								LSB								MSB							
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	GREEN(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
BLUE	BLUE(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	BLUE(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0
	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0

[Note]

1) Definition of gray scale:

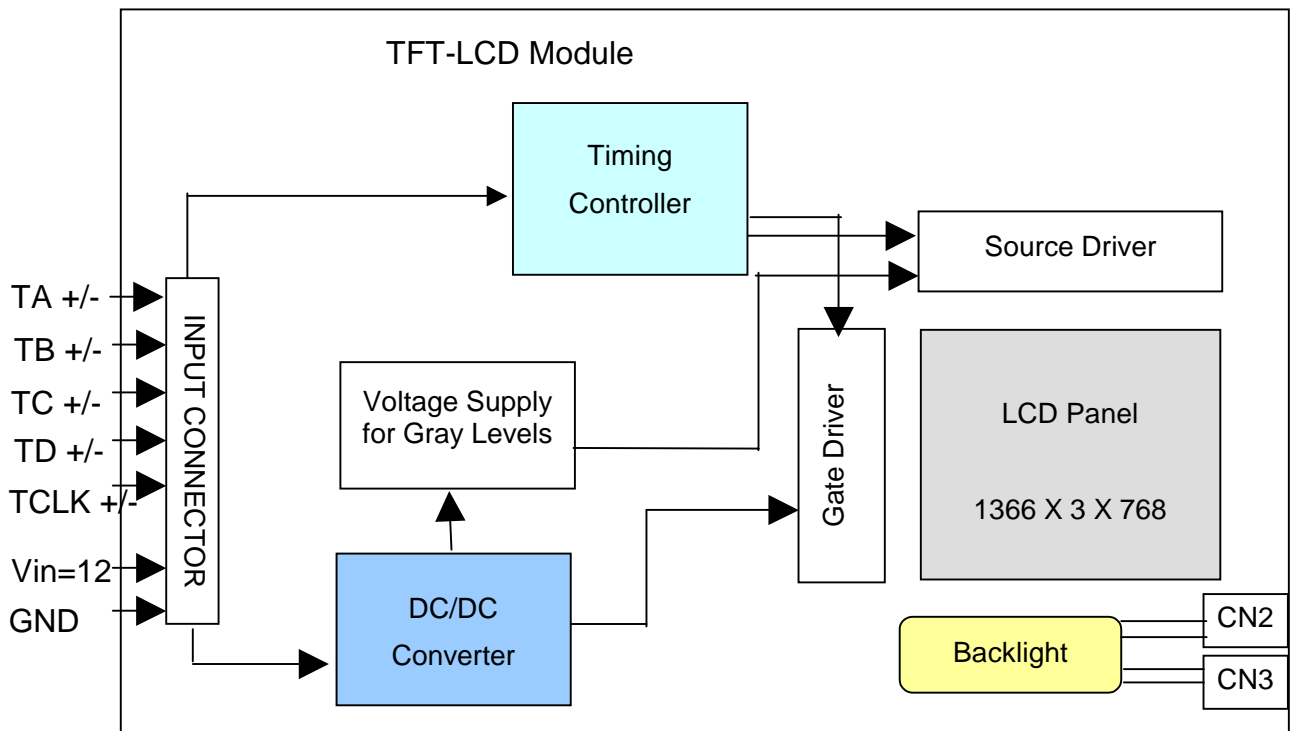
Color (n): n indicates gray scale level, higher n means brighter level.

2) Data: 1-High, 0-Low

5.6 DATA MAPPING

D(1, 1)	D(2, 1)	---	D(X, 1)	---	D(1365, 1)	D(1366, 1)
D(1, 2)	D(2, 2)	---	D(X, 2)	---	D(1365, 2)	D(1366, 2)
⋮	⋮	+	⋮	+	⋮	⋮
D(1, Y)	D(2, Y)	---	D(X, Y)	---	D(1365, Y)	D(1366, Y)
⋮	⋮	+	⋮	+	⋮	⋮
D(1,767)	D(2,767)	---	D(X,767)	---	D(1365,767)	D(1366,767))
D(1,768)	D(2,768)	---	D(X,768)	---	D(1365,768)	D(1366,768)

6. BLOCK DIAGRAM



BACKLIGHT UNIT

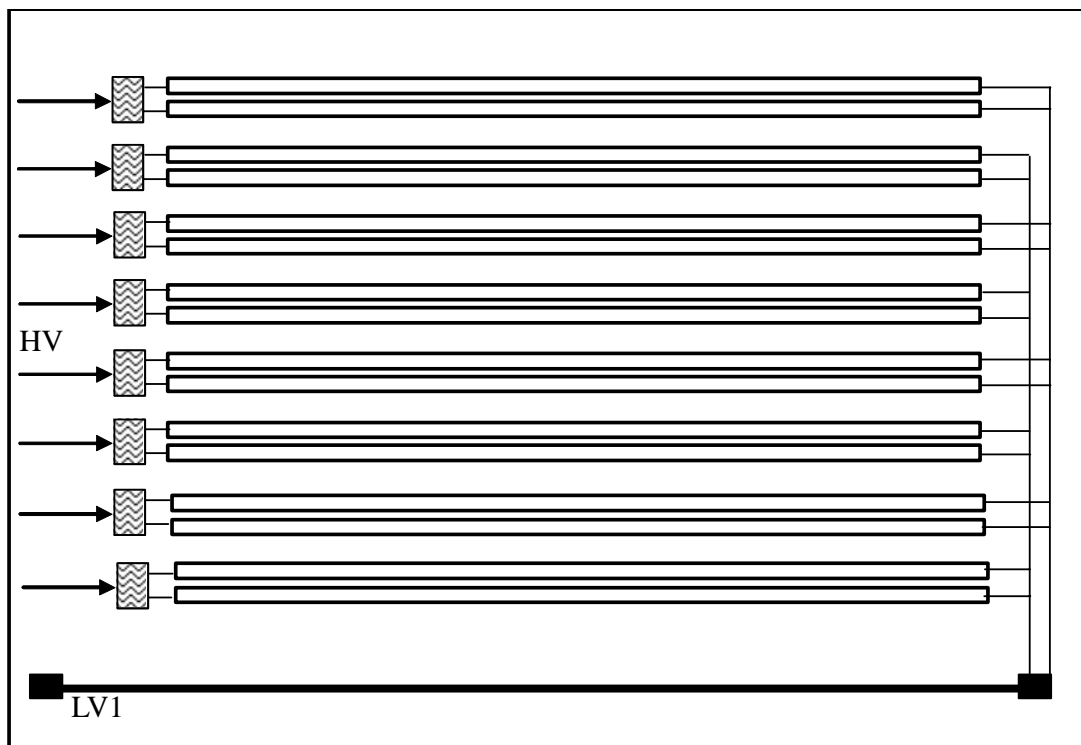
Lamp connector

HV: BHR-02VS-1(JST)*8 or compatible

Mating connector: SM02 (8.0)B-BHS-1-TB (JST) or compatible

LV1: BHR-02VS-1(JST)*1 or compatible

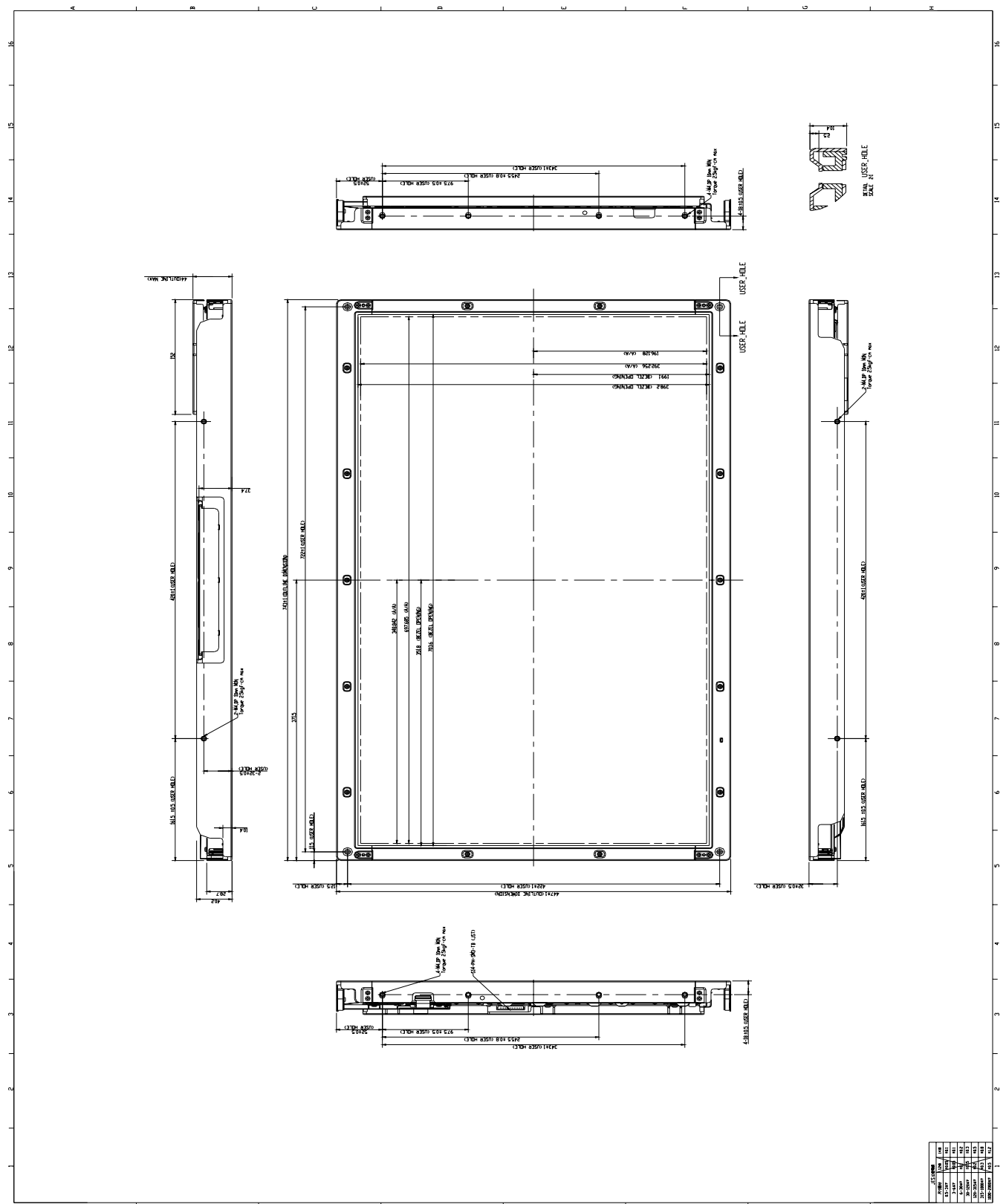
Mating connector: SM02 (8.0)B-BHS-1-TB (JST) or compatible



7. MECHANICAL SPECIFICATION

7.1 FRONT SIDE

(include Inverter, if the dimension did not to eerance, please refer to the table.) [Unit: mm]



(include Inverter, if the dimension did not to eerance, please refer to the table.) [Unit: mm]



8.OPTICAL CHARACTERISTICS

Ta = 25°C, VCC=12V

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARKS
Contrast (CEN)		CR	$\theta = \psi = 0^\circ$ Point-5	700	1000	--	--	*1)*2)*3)
Luminance	Central luminance	Lwc	$\theta = \psi = 0^\circ$	450	550	--	cd/m ²	*9)
	5P Luminance (AVG)	Lw9	$\theta = \psi = 0^\circ$	--	500	--	cd/m ²	*2)*3)
	Uniformity	ΔLw	$\theta = \psi = 0^\circ$	75	--	--	%	*2)*3)
Response Time (White – Black)		tr	$\theta = \psi = 0^\circ$	--	10	(17)	ms	*3)*4)
		tf	$\theta = \psi = 0^\circ$		6	(8)	ms	*3)*4)
Response Time (Gray to gray average)		trg, tfg		--	10	(15)	ms	*5)
Image sticking		tis	4 h	--	--	(3)	sec	*6)
View angle	Horizontal	ψ	$CR \geq 10$ Point-5	-80~80	-85~85	--	°	*2)*3)
	Vertical	θ		-80~80	-85~85	--	°	*2)*3)
Crosstalk Ratio		CMR	$\theta = \psi = 0^\circ$	--	--	(1)	%	*3)*7)
Color Chromaticity	Red	Rx Ry	$\theta = \psi = 0^\circ$ Point-5	TBD	TBD	TBD	--	*2)*3)
	Green	Gx Gy		TBD	TBD	TBD		
	Blue	Bx By		TBD	TBD	TBD		
	White	Wx Wy		TBD	0.283 0.297	TBD		
Color Temperature		Tc		--	9300	--	K	*3)
Color Gamut		CG		--	75	--	%	*8)

[Note]

These items are measured using: BM-5A (TOPCON)

View angle: EZ contrast XL-88, Response Time: Westar TRD-100

[under the dark room condition (no ambient light).]

Definition of these measurement items is as follows:

- *1) Definition of Contrast Ratio: [These items are measured using BM-5A (TOPCON) under the dark room condition (no ambient light).]

CR=ON (White) Luminance/OFF (Black) Luminance

- *2) Definition of Luminance, Luminance uniformity, Contrast, and the Deviation of Color Coordinate:

Luminance and Contrast: To measure at the center position “5” on the screen (NO.5), see Figure.8-1 below.

Luminance uniformity: Lw (MAX) and Lw(MIN) are the maximum and minimum luminance value measure at the position “1~5” on the screen (NO.1~5), see Figure.8-1 and below show equation:

$$\Delta Lw = [(Lw(MIN)) / Lw(MAX)] \times 100\%$$

The Deviation of Color Coordinate: To measure at the position “1~5” on the screen (NO.1~5), see Figure.8-1 below.

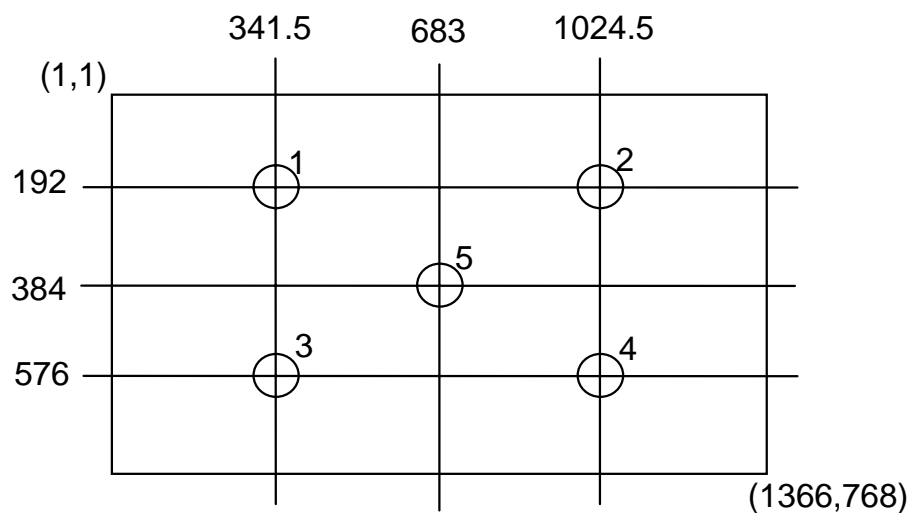


Figure 8-1. Measurement Positions

*3) Definition of Viewing Angle (θ , ϕ):

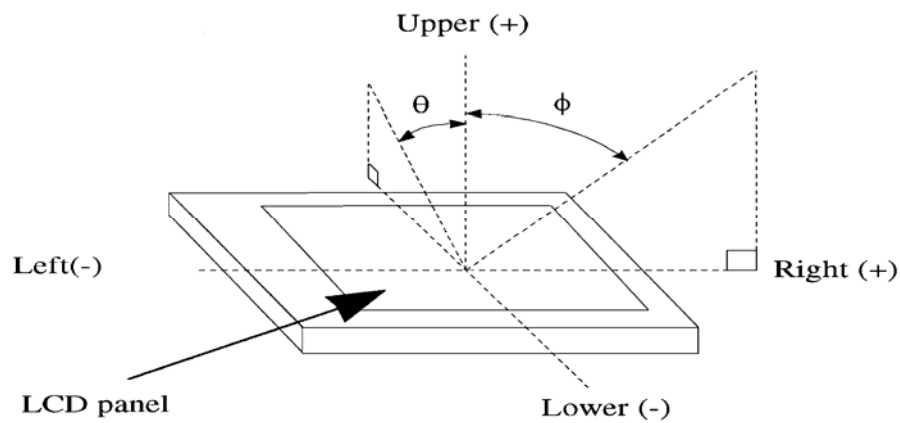


Figure 8-2. Definition of Viewing Angle

*4) Definition of Response Time (White – Black)

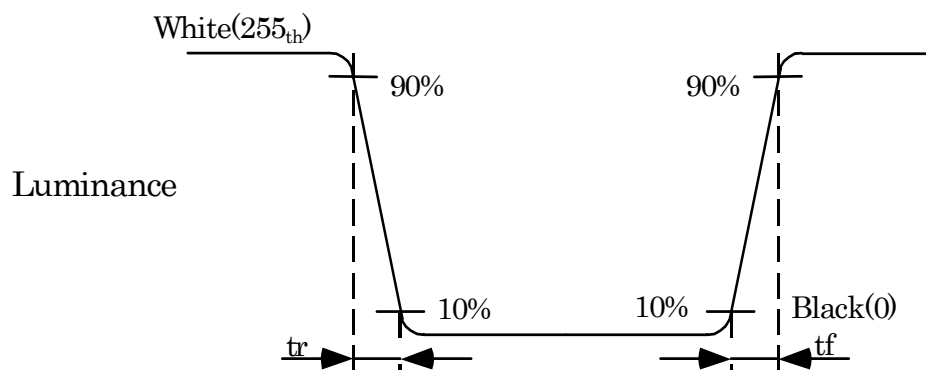


Figure 8-3. Definition of Response Time (White – Black)

*5) Definition of Response Time (Gray to Gray, Average)

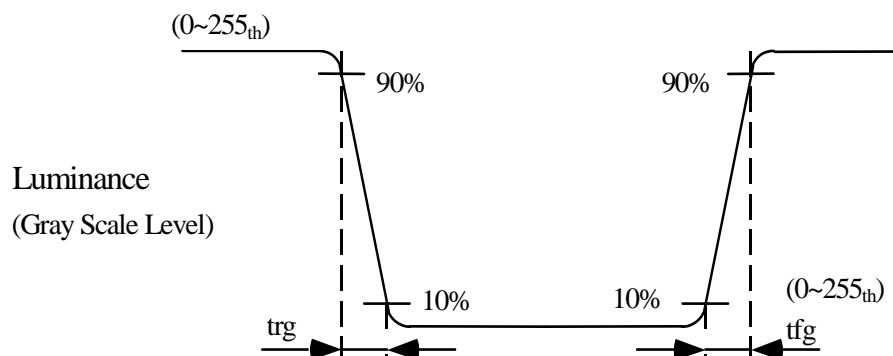


Figure 8-4. Definition of Response Time (Gray to Gray)

The driving signal time means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223, 255. Gray to gray average means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223, 255 to each other.

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed

after lighting Backlight for 1 hour in a windless room.

***6) Image Sticking Test Method:**

Continuously display the test pattern shown in the figure below for specified time. To change the module frame to gray pattern (gray 120 pattern), and it's displaying grade still under specification.

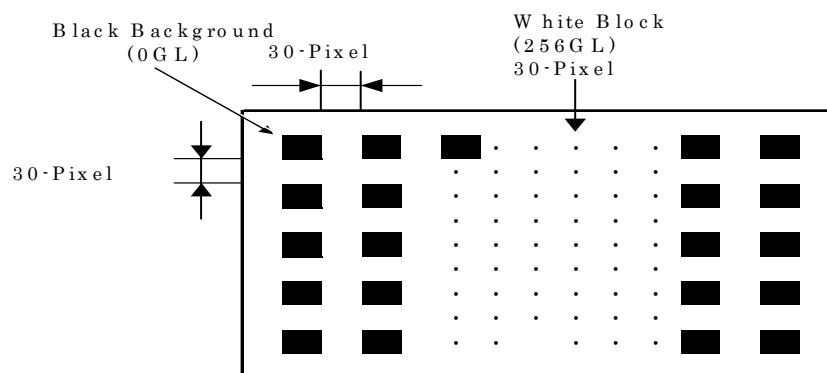


Figure 8-5. The Pattern of Image Sticking Test

*7) Definition of Cross talk Ratio

$$CMR = \text{MAX} ((| (LB1-LA) / LC |) \times 100\% , (| (LB2 - LA) / LC |) \times 100\%)$$

LA: Pattern A (Half-Tone pattern) Measure point Luminance

LB1, LB2: Pattern B1, Pattern B2 Measure point Luminance

LC: Pattern C (white pattern) Measure point Luminance

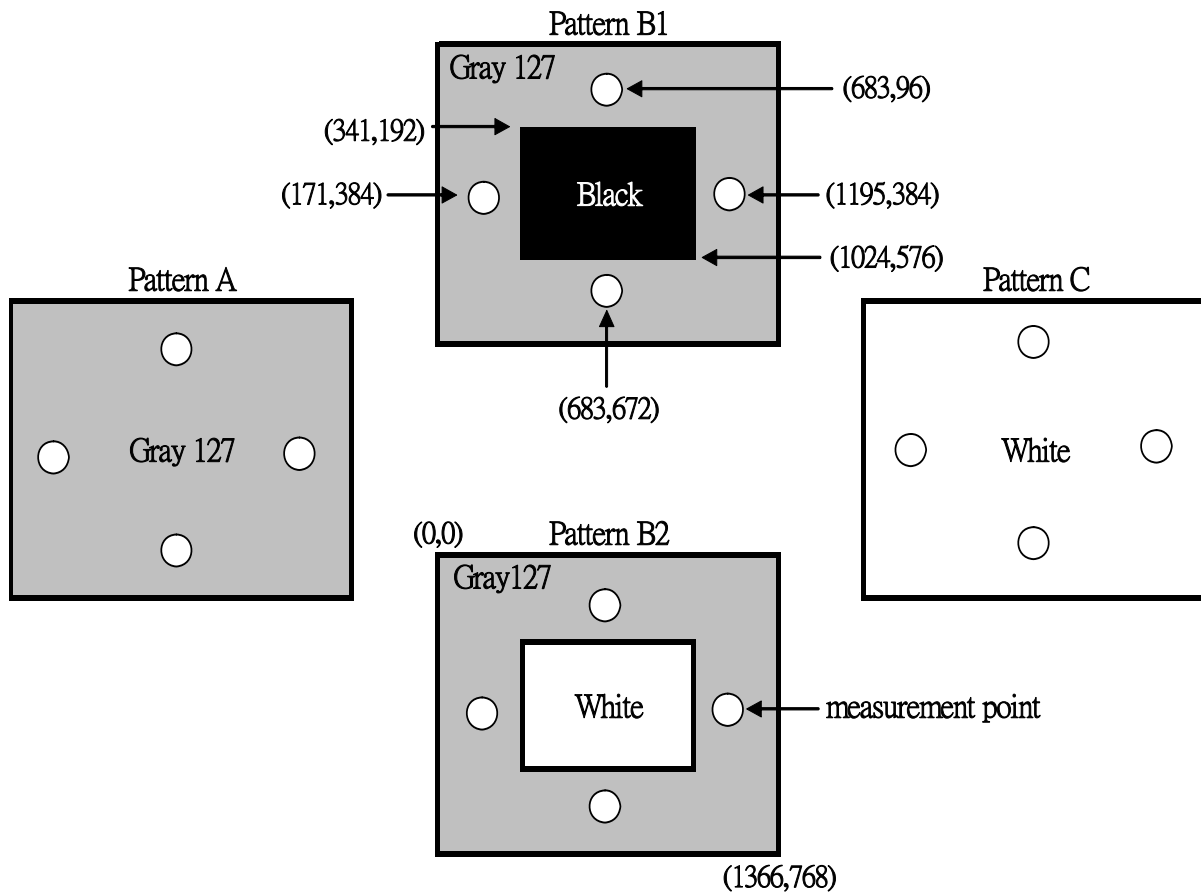


Figure 8-6. The Pattern of Cross talk Test

*8) Definition of Color Gamut:

To measure RGB three sub-pixels color gamut coordinate at CIE coordinate chart from the center of module, to form a triangle area = A_{RGB} .

RGB three sub-pixels of NTSC at CIE coordinate chart to form a triangle area = N_{RGB} .

$$CG = \frac{A_{RGB}}{N_{RGB}} \times 100$$

*9) Definition of Central luminance:

After lighting on the panel for 30 mins, then the Central luminance test proceeded. The definition of TYP value is under status of Inverter Dimming Voltage=5V.

9.RELIABILITY TEST CONDITIONS

9.1 TEMPERATURE AND HUMIDITY

TEST ITEMS	CONDITIONS
High Temperature Operation	50°C; 240hrs
High Temperature Storage	60°C; 240hrs
High Temperature High Humidity Operation	50°C; 90% RH; 240 hrs (No condensation)
Low Temperature Operation	0°C; 240 hrs
Low Temperature Storage	-20°C; 240 hrs

9.2 SHOCK AND VIBRATION

ITEMS	CONDITIONS
Shock (Non-Operation)	Shock level: 980m/s ² (100G) Waveform: half sinusoidal wave, 2ms Number of shocks: one shock input in each direction of three mutually perpendicular axes for a total of six shock inputs.
Vibration (Non-Operation)	Vibration level: 9.8m/s ² (1.0G) zero to peak Waveform: sinusoidal Frequency range: 10 to 300 Hz Frequency sweep rate: 0.5 octave/min Duration: one sweep from 10 to 300Hz in each of three mutually perpendicular axis (each x, y, z axis:10 min, total 30 mins)

9.3 JUDGMENT STANDARD

The judgment of the above test should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect.

Partial transformation of the module parts shall be ignored.

Fail: No display, obvious non-uniformity, or line defects.

10. PACKAGING

10.1 PACKING SPECIFICATIONS

- (1) 3 LCD TV modules/1 Box
- (2) Box dimensions: 975(L) x 375(W) x 562(H)
- (3) Weight: approximately 31.9kg (3 modules per box)

10.2 PACKING METHOD

Figure 1 and Figure 2 are the packing method.

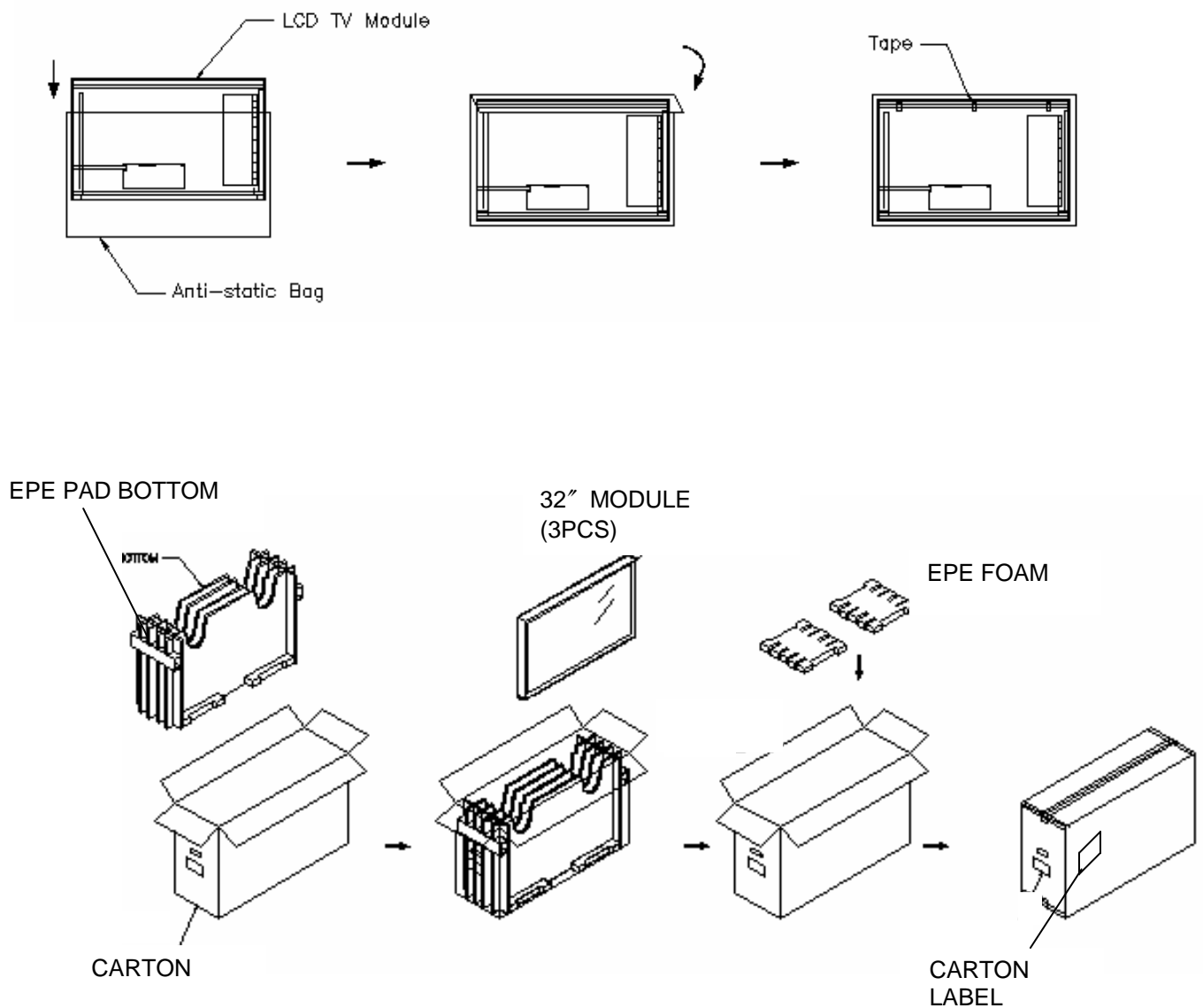


Figure 1 Packing Method

-
- (1) Corner protector: L1125 x 50mm x 50mm
 - (2) Pallet: L1000 x W1150 x H130mm
 - (3) Bottom Cap: 1000 x W1150 x H130mm
 - (4) Pallet Stack: 1000 x W1150 x H1250mm
 - (5) Gross: 273kg

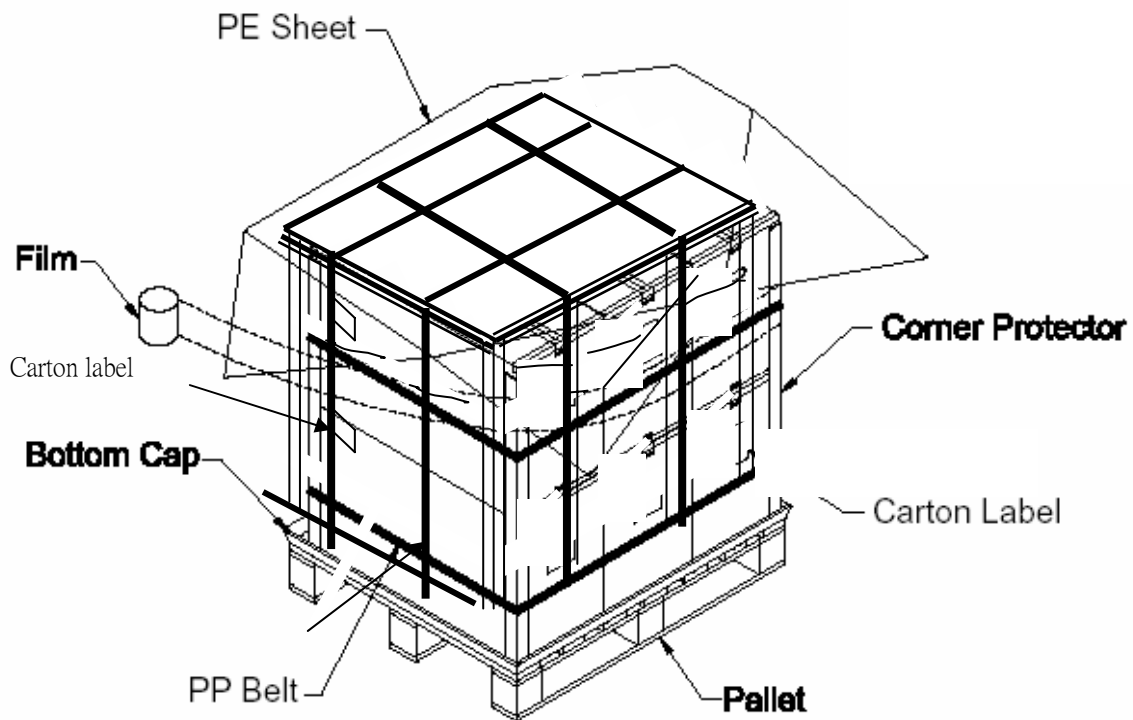


Figure 2 Packing Method

11. HANDLING PRECAUTIONS FOR TFT-LCD MODULE

Please pay attention to the followings in handling TFT-LCD products.

11.1 ASSEMBLY PRECAUTION

- (1) Please use the mounting hole on the module side in installing and do not beading or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.
 - (2) Please design display housing in accordance with the following guidelines.
 - Housing case must be destined carefully and do not to put stresses on LCD all sides or wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.
 - Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. Approximately 1.0 mm of the clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.
 - When some parts, such as, FPC cable and ferrite plate, are installed underneath the LCD module, still sufficient clearance is required, such as 0.5mm. This clearance is, especially, to be reconsidered when the additional parts are implemented for EMI countermeasure.
 - Design the inverter location and connector position carefully so as not to put stress on lamp cable.
 - Keep sufficient clearance between LCD module and the other parts, such as inverter and speaker so as not to interface the LCD module. Approximately 1.0mm of the clearance in the design is recommended.
 - (3) Please do not push or scratch LCD panel surface with any-thing hard. And do not soil LCD panel surface by touching with bare hands. (Polarizer film and surface of LCD panel are easy to be flawed.)
 - (4) Please do not press any parts on the rear side such as source TCP, gate TCP, control circuit board and FPC during handling the LCD module. If pressing rear part could not be avoided, handle the LCD module with care not to damage them.
 - (5) Please wipe out LCD panel surface with absorbent cotton or soft clothe in case of it being soiled.
 - (6) Please wipe out drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.
 - (7) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
 - (8) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
-

-
- (9) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with inverter.

11.2 OPERATING PRECAUTIONS

- (1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
- (2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification.
- (1) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.
- (2) A condensation might happen on the surface and inside of LCD module in case of sudden change of ambient temperature.
- (3) Please pay attention to displaying the same pattern for a very long time. Image might stick on LCD. If then, time going on can make LCD work well.
- (4) Please obey the same caution descriptions as ones that need to pay attention to ordinary electronic parts.

11.3 PRECAUTIONS WITH ELECTROSTATICS

- (1) This LCD module use CMOS-IC on circuit board and TFT-LCD panel, and so it is easy to be affected by electrostatics. Please be careful with electrostatics by the way of your body connecting to the ground and so on.
- (2) Please remove protection film very slowly on the surface of LCD module to prevent from electrostatics occurrence.

11.4 STORAGE PRECAUTIONS

- (1) When you store LCD for a long time, it is recommended to keep the temperature between 0°C ~40°C without the exposure of sunlight and keep the humidity less than 90%RH.
- (2) Please do not leave the LCD in the environment of high humidity and high temperature such as 60°C 90%RH.
- (3) Please do not leave the LCD in the environment of low temperature(can not lower than -20°C).

11.5 SAFETY PRECAUTIONS

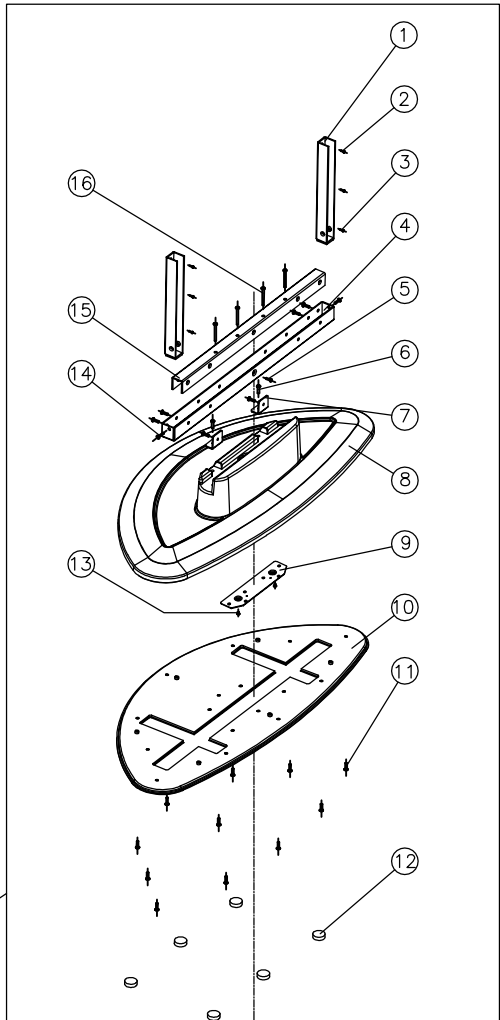
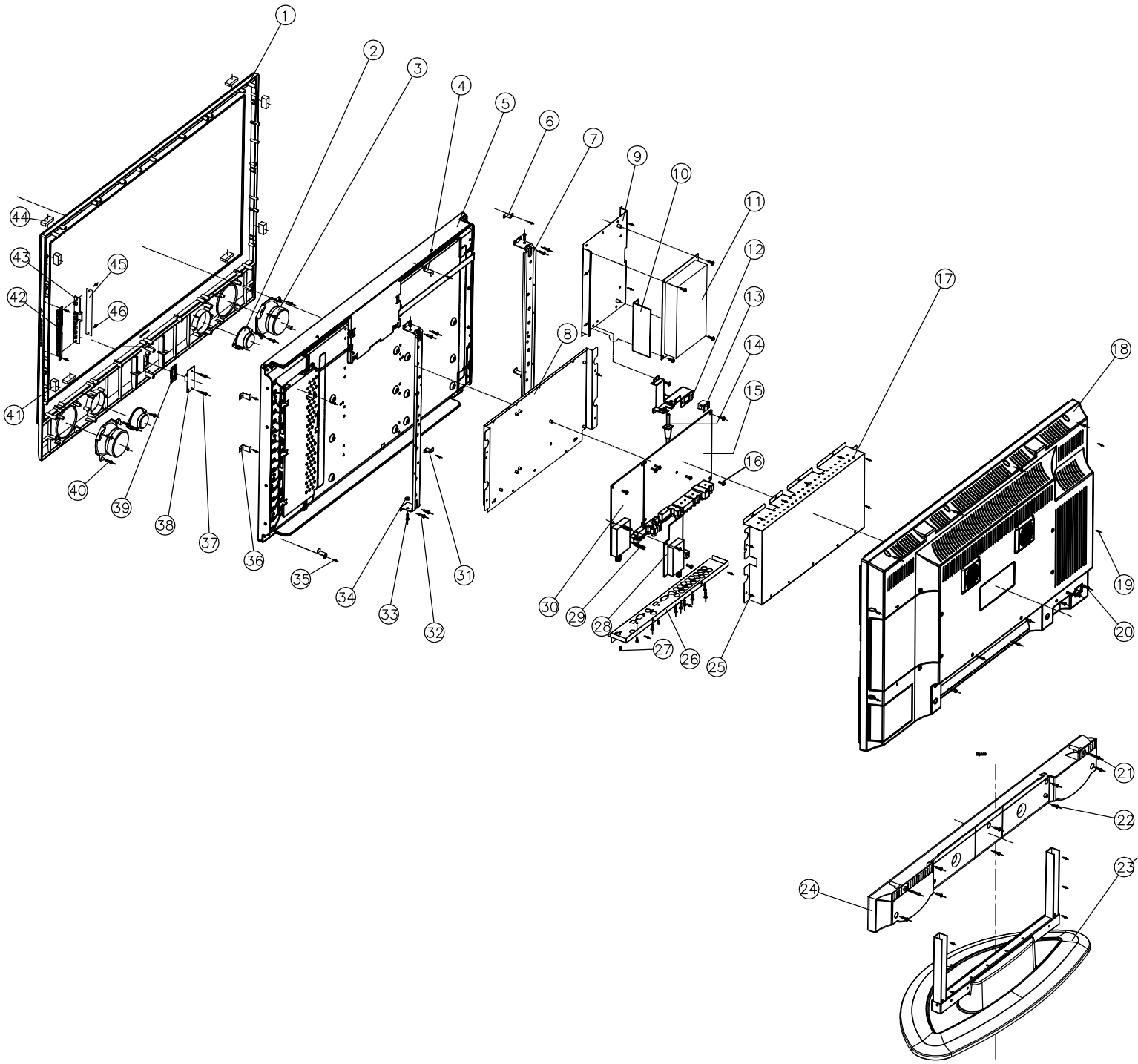
- (1) When you waste LCD, it is recommended to crush damaged or unnecessary LCD into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- (2) If any liquid leaks out of a damaged-glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

11.6 OTHERS

- (1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight and strong UV rays.
- (2) Please pay attention on the side of LCD module do not contact with other materials in preserving it alone.
- (3) For the packaging box, please pay attention to the followings:
 - Packaging box and inner case for LCD are designed to protect the LCD from the damage or scratching during transportation. Please do not open except picking LCD up from the box.
 - Please do not pile them up more than 3 boxes. (They are not designed so.) And please do not turn over.
 - Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
 - Packing box and inner case for LCD are made of cardboard. So please pay attention not to get them wet. (Such as keep them away from high humidity or wet place.)

NOTE : THIS RELEASED DRAWING WAS PRODUCED BY COMPUTER , DO NOT UPDATE MASTER MANUALLY

DWG. REV.	ZONE	DESCRIPTION	DATE	REVISOR



16	603-407040-00	MACH. SCREW TRS. M4X40MM	4	
15	429-L32AB36-01	U TOP CROSSBEAM	1	SECC T=2
14	602-407008-00	MACH.SCREW WASHER 4X8	12	
13	614-300108-00	S-TAP. SCREW 3X8	2	
12	370-42D101-01	RUBBER FOOT	6	RUBBER
11	610-350210-10	S-TAP.SCREW 3.5X10	11	
10	429-L32AB11-01	BASE SHEET	1	SECC T=1.0
9	429-L32AB09-01	SECURE SHEET	1	SECC T=1.0
8	231-L32AB21-01R	BASE COVER	1	HIPS
7	429-L32AB03-01	L SHEET	2	SECC T=2
6	604-407012-00	MACH.SCREW M4X12	2	
5	601-407010-00	MACH.SCREW M4X10	1	
4	429-L32AB35-01	U BOTTOM CROSSBEAM	1	SECC T=2
3	604-407016-00	MACH.SCREW M4X16	4	
2	614-400412-00	S-TAP. SCREW BID 4X12	2	
1	429-L32AD13-011	SECURE LEG	2	SECC T=2.0
IETM	PART NO.	DESCRIPTION	QTY	MATERIAL

46	614-220206-10	S-TAP. SCREW BID 2.2X6	2	
45	384-L32AD03-01H	PVC SHEET FOR KEY	1	PVC
44	379-L32SD02-01Y	RUBBER CUSHION-B	4	RUBBER
43	771KL37AD01-01	FUNCTION KEY PCB ASSY	1	
42	277-L32AD11-00S	FUNCTION KEY	1	ABS
41	379-L32SD01-01Y	RUBBER CUSHION-A	4	RUBBER
40	612-300110-10	S-TAP.SCREW WHR 3X10	12	
39	269-42SD01-01L	REMOTE RECEIVE LENS	1	ABS
38	771BL37AD01-01	REMOTE PCB	1	
37	614-260208-10	S-TAP. SCREW BID 2.6X8	4	
36	429-L32SD03-01	Z BKT FOR PANEL-A	2	SECC T=1.0
35	429-L32SD04-01	Z BKT FOR PANEL-B	4	SECC T=1.0
34	530-100053-15	FIBBER WASHER	4	
33	604-407008-10	TAPTITE SCREW 4X8 BS	4	
32	614-400110-10	SELF TAPPING SCREW	8	
31	429-L32SD05-01	Z BKT FOR PANEL-C	2	SECC T=1.0
30	771S42D102-01	ATSC TUNER PCB ASSY	1	
29	649-42AA02-01	CONNECTION BOSS	2	
28	771L37AD01-01	NTSC TUNER PCB ASSY FOR LCD37	1	
27	624-204005-10	S-TAP. SCREW BID 2.0X5	1	
26	436-L32AB08-01S	RERMINAL SHEET	1	SECC T=0.8
25	604-305005-10	MACH.SCREW BID 3X8	15	
24	206-L32AD01-00R	SPEAKER CABINET BACK	1	HIPS
23	734-L32AD03-01	BASE ASSY		
22	614-400416-00	S-TAP.SCREW BID 4X16	14	
21	614-400445-00	S-TAP. SCREW BID M4X45	2	
20	601-305008-00	MACH.SCREW CTS 3X8	8	
19	610-300115-00	S-TAP. SCREW ROUND3X15	4	
18	202-L32AD22-01AV	BACK CABINET	1	HIPS(94V0)
17	483-L32AB22-01S	SHIELD COVER(VSC)	1	SPT E T=0.3
16	602-305006-10	MACH. SCREW WHE 3X6	14	
15	771EL37AD02-01	MAIN PCB ASSY	1	
14	E3404-157009	AC CORD UL 1.88M FOR LCD32 M78202	1	
13	E4101-027001	SWITCH	1	
12	426-L32AD02-01S	POWER CORD BKT.	1	SECC T=0.8
11	E7801-P02002	POWER ASSY	1	
10	384-L32AD02-01H	PVC SHEET FOR POWER	1	PVC
9	481-L32AD01-01S	POWER SHIELDING BOTTOM	1	SECC T=0.8
8	481-L32AB06-01S	SHIELDING BOX(VSC)	1	SECC T=0.8
7	420-L32AD02-01S	MINA SUPORT	2	SECC T=1.5
6	429-L32SD04-01	Z BKT FOR PANEL B	4	SECC T=1.0
5	E6203-32TD02	PANEL ASSY-CPT	1	
4	429-L32AS0A-01	Z BKT. FOR PANEL	1	SECC T=1.0
3	E4801-124001	BOURDON SPEAKER	2	
2	E4802-014001	ALT SPEAKER	2	
1	200-L32AD02-01AAV	FRONT CABINET	1	HIPS(94V0)
IETM	PART NO.	DESCRIPTION	QTY	MATERIAL

DRAWN.	LCQ					TOLERANCE UNLESS OTHERWISE SPECIFIED	KAWA	ELECTRONIC R & D CENTRE	TITLE	LCT3285TA-EXP-CPT
CHECKED						0: ±0.30 0.0 ±0.10 0.00: ±0.05	MATL.		MODEL NO.	LC32HAD
APPRD.						ANGULAR: ±0.3°	FINISH		A3	PART NO.
3rd ANGLE PROJECTION						UNIT : mm			DWG. NO.	
									SCALE	QTY.
										SHEET 1 OF 1

Spare Part List for LCT3285TA

Item	Part Number	Part Description	Usage / unit	Unit	Key/Spare
	LCT32ADNIA1TS-A01	AKAI LCD32"(LCT3285TA) S-MT8202+CPT AC120V/60HZ USA SILVER			
1>	510-L32AD01-02AKA	CARTON BOX AKAI LCT3285TA (MTK-8202) K	1	Piece	K
2>	580-L32ADHS-TU03L	IB E FOR AKAI LCT32AD USA CPT(CLAA32WA01) S-MTK8202	1	Piece	K
3>	E7501-056102	REMOTE CONTROL K001 "AKAI" 44KEYS MT8202 LCD32"/27" (W/O DVD) USA SILVER/BLACK	1	SET	K
4>	771EL37AD02-01	PCB ASSY MAIN S-MT8202 FOR 37LCD CPT	1	SET	K
5>	771L37AD01-01	NTSC TUNER PCB ASSY FOR LCD37	1	SET	K
6>	771S42D102-01	ATSC TUNER PCB ASSY	1	SET	K
7>	200-L32AD02-01AAV	CABINET FRONT SIL/BLK CPT PANEL AV	1	Piece	S
8>	202-L32AD22-01AV	CABINET BACK BLACK	1	Piece	S
9>	206-L32AD01-01RV	SPEAKER CABINET BACK BLACK LCT32AD R	1	Piece	S
10>	269-42SD01-01L	REMOTE RECEIVE LENS	1	Piece	S
11>	277-L32AD11-01S	FUNCTION KEY SIL(MATERIAL:BLACK) LCT32SD	1	Piece	S
12>	300-L32AD14-02C	POLYFOAM TOP L32AD C	1	Piece	S
13>	300-L32AD15-02C	POLYFOAM BOTTOM	1	Piece	S
14>	310-111404-07V	POLYBAG 11"X14"X0.04 FV	1	Piece	S
15>	310-423850-07V	BAG LAMIFILM 42"X38"X0.5MM	1	Piece	S
16>	384-L32AD02-01H	PVC SHEET FOR POWER 230X180X0.5 H	1	Piece	S
17>	384-L32AD03-01H	PVC SHEET FOR KEY	1	Piece	S
18>	387-L32AD01-01AHA	MODEL PLATE AKAI LCT3285TA H	1	Piece	S
19>	426-L32AD02-01S	POWER CORD BRACKET ASSY	1	Piece	S
20>	436-L32AB0B-01S	TERMINAL SHEET MT8202 TV	1	Piece	S
21>	481-L32AB06-01S	SHIELDING BOTTOM MT8202	1	Piece	S
22>	481-L32AD01-01S	SHIELD BOX FOR POWER L32AD S	1	Piece	S
23>	483-L32AB22-01S	SHIELDING COVER	1	Piece	S
24>	486-M32111-01	NAME PLATE M AKAI	1	Piece	S
25>	521-300055-01	FELT PAPER 300X5X0.5MM	4	Piece	S
26>	522-421D01-01	MASKING PAPER	1	Piece	S
27>	530-100053-15	FIBBER WASHER 10.0X5.3X1.5MM W/ADHESIVE	4	Piece	S
28>	563-119-	SERIAL NO. LABEL	1	Piece	S
29>	568-P46T02-02	WARNING LB ENG 42SF NIL	1	Piece	S
30>	579-42D102-09	SERIAL NO/BAR CODE LABEL 42D1	1	Piece	S
31>	579-42D103-02	ON/OFF LB ENG 42D1 NIL	1	Piece	S
32>	579-42D105-01	PROTECTIVE EARTH LABEL FOR ESA 42TD1	1	Piece	S
33>	579-L27AD09-01	CAUTION LABEL ENG AKAI	1	Piece	S

Spare Part List for LCT3285TA

Item	Part Number	Part Description	Usage / unit	Unit	Key/Spare
34>	579-L32AD02-02APA	UPC LABEL LCT3285TA P	2	Piece	S
35>	590-L32AD01-02	WARRANTY CARD AKAI LCT3285TA	1	Piece	S
36>	593-L32AD01-03	INSERTION CARD LCT3285TA MTK8202	1	Piece	S
37>	E3404-157009	AC CORD UL 1.88M FOR LCD32 MT8202	1	Piece	S
38>	E3421-924009	WIRE ASSY 2P L120	2	Piece	S
39>	E3421-925127	WIRE ASSY TJC3-2Y L860 SPK-R MT8202	1	Piece	S
40>	E3421-925129	WIRE ASSY 10P/2.5 FOR MT8202 27" POWER 9V/12V	1	Piece	S
41>	E3421-925130	WIRE ASSY 1H3.96-2KN6 20 L180 2P FOR LCD32"/27"	2	Piece	S
42>	E3421-925133	WIRE ASSY TJC3-3Y L650 SPK-L MT8202	1	Piece	S
43>	E3421-926119	WIRE ASSY P2.0 8P L=215 TV/SIF	1	Piece	S
44>	E3421-926125	WIRE ASSY P2.5 4P/4P L400MM AMP24V EMI MT8202	1	Piece	S
45>	E3461-064038	WIRE ASSY P2.5 7P/7P L400MM 5V STANBY POWER MT8202 FOR 27"/32" LCD	1	Piece	S
46>	E3461-064040	WIRE ASSY P2.0 14P/3P2.0/8P2.5 L400MM/L700MM INVERTER MT8202	1	Piece	S
47>	E3471-000044	WIRE WS SHIELD WIRE FOR 32LCD COMBO MICO KEY 13P/8P+5P	1	Piece	S
48>	E3471-001002	WIRE WS SHIELD P1.0 0P L=220 FOR CPT LCD37"	1	Piece	S
49>	E4101-027001	SWITCH POW MR-22-N2BB-F2 ROCKET	1	Piece	S
50>	E4801-124001	SPEAKER 8 OHM 10W D3" YD78-1	2	Piece	S
51>	E4802-014001	TWEETER 6 OHM 10W D2" YD52-1	2	Piece	S
52>	E6203-32TD02	DISPLAY LCD 32" CPT WXGA CLAA320WA01C 1366X768 550CD/M2	1	Piece	S
53>	E7301-010002	BATTERY AAA R03P1.5V <2>	2	Piece	S
54>	E7801-P02002	PCB ASSY PSU BOARD MEGMEET MT169 FOR 32LCD AC110-240V OUTPUT 12V/8V/24V 220W	1	SET	S
55>	734-L32AD03-01	PLASTIC BASE ASSY LCT3201TD W/O LOGO W/O PACKING SILVER	1	SET	S
56>	771BL37AD01-01	IR RECEIVE PCB ASSY FOR LCT37AD	1	SET	S
57>	771KL37AD01-01	KEY PCB ASSY FOR LCT37AD	1	SET	S

Software Upgrade

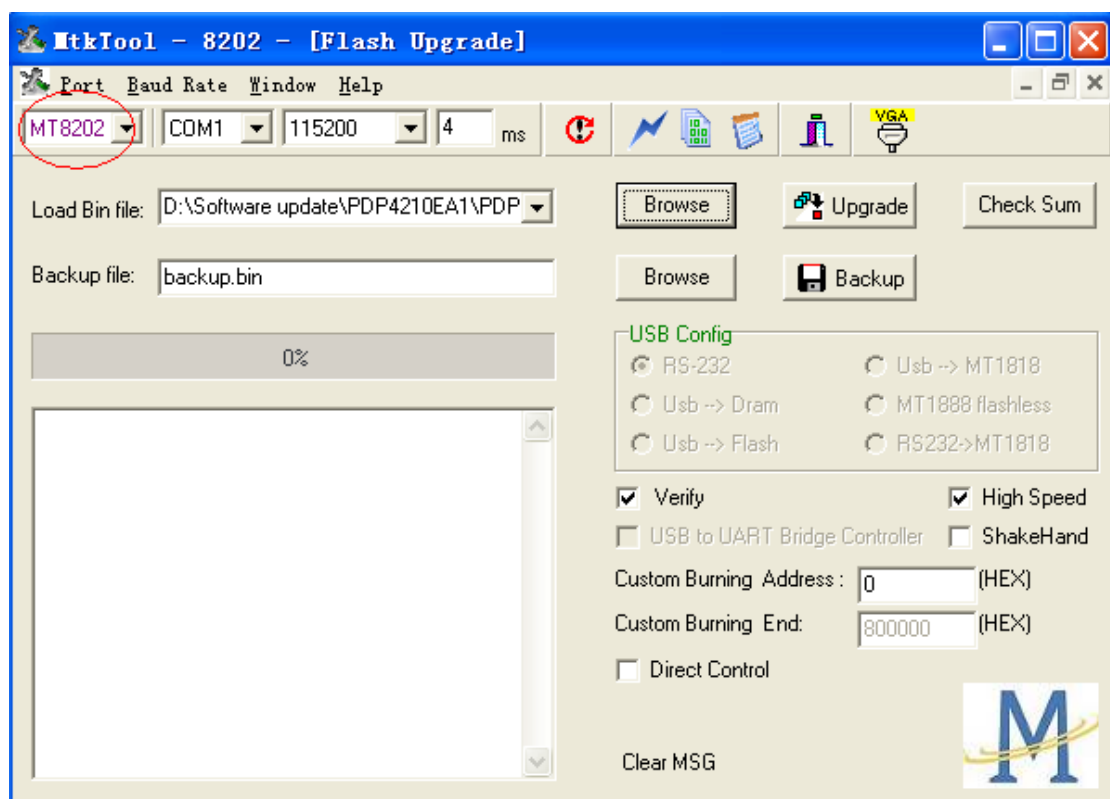
Process of update MT8202

Preparing :

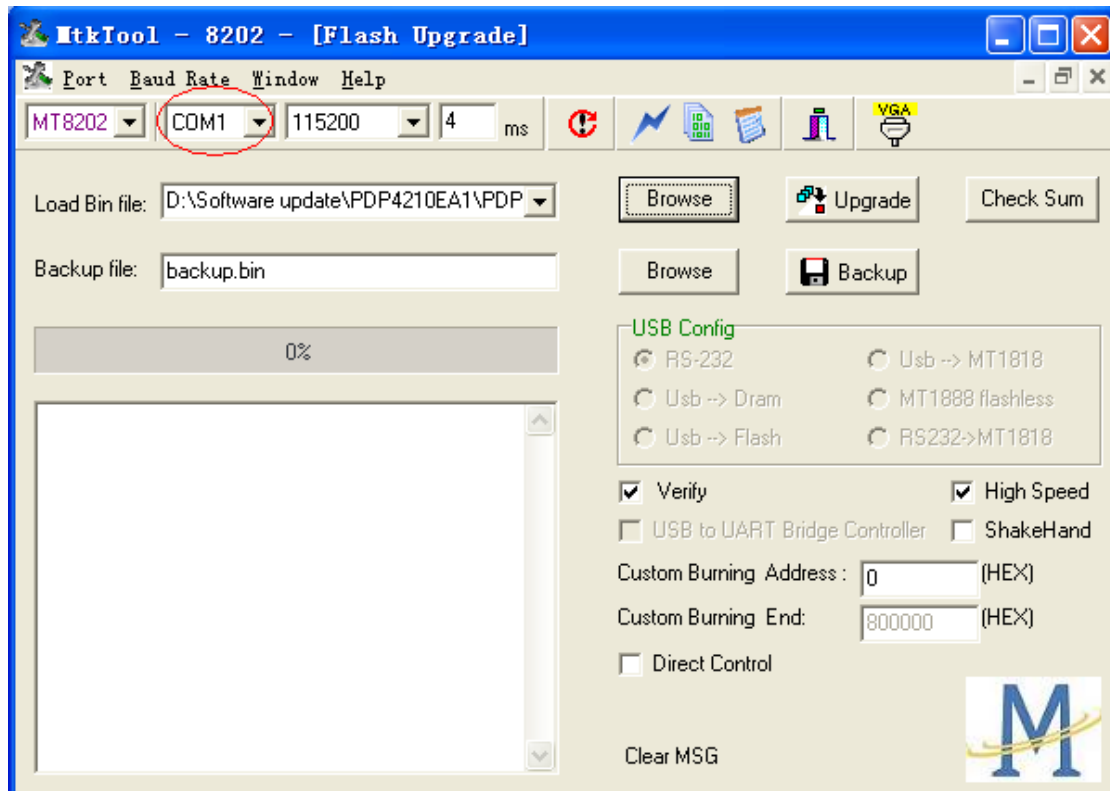
1. Connect **RS232-VGA download line**, One connector is connected to **VGA connect port of Plasma TV** ,while another side is connected to PC COM port.
2. Store the MtkTool into the PC .

Downloading :

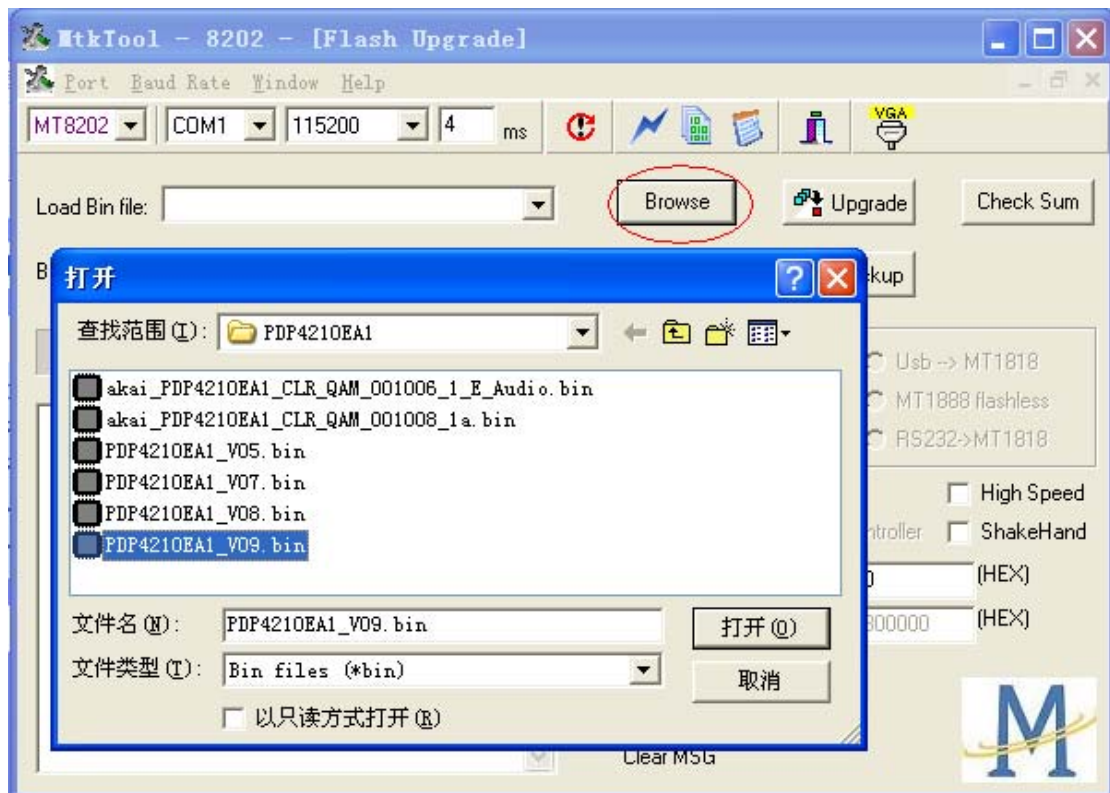
3. Turn on AC power switch of the Plasma TV and then press the button “standby” of the remote control . The image could be found on the screen of the Plasma TV while the color of the power indicator is green . (the mode of the Plasma TV will be standby mode if after turn on the main power switch only .)
4. Execute MTKtool and select the chipset as MT8202. (the software of MTKtool will be sent to your side)



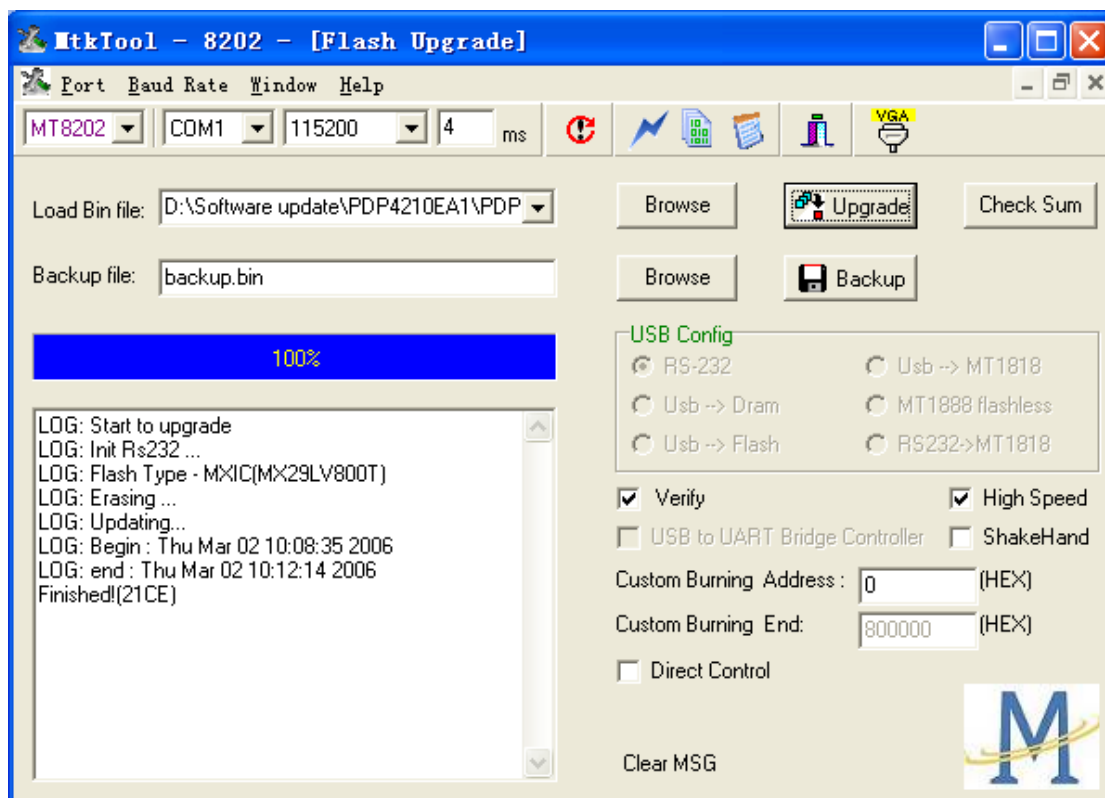
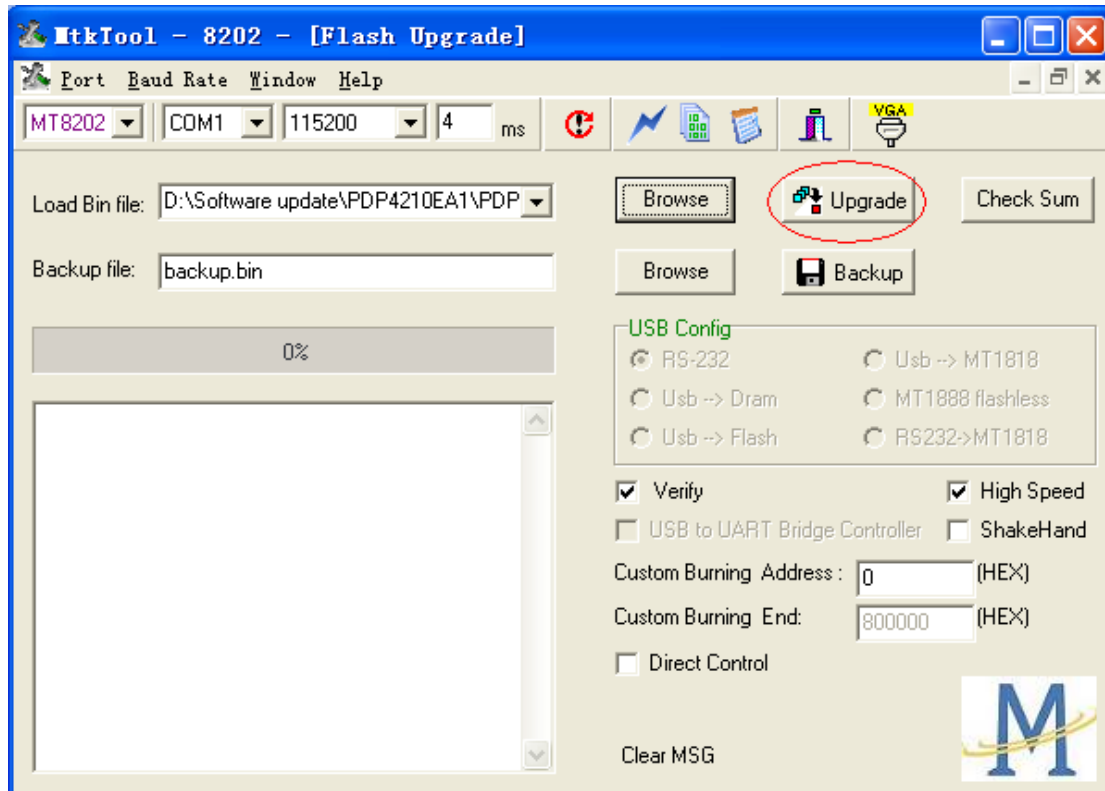
5. Select current COM port. (please try to check the COM port of your PC).



6. Choose the bit rate as 115200.
7. Select the update binary by pressing browse button. For example, the binary file name is PDP4210EA1_V09.bin. (this update firmware will be sent to your side)



8. Press Upgrade button and start update process.



9. The update process is successful as the progress bar is 100%. After the update process is ok,

turn off power and wait indicator light is off. Turn on power and TV can work.

Checking

It is needed to check the version of the firmware for MT8202 which has been download into the Plasma TV .

Press Menu button of the remote control, following input “8202” of the remote control and OSD menu for Factory Setting is appeared on the screen .

Use the remote control and select the mode of Firmware Version and then enter the mode of Firmware Version . It is easy to be found the version of the current firmware for MT8202 is as the following : “Factory ID : PDP4210EA1_VXX ”

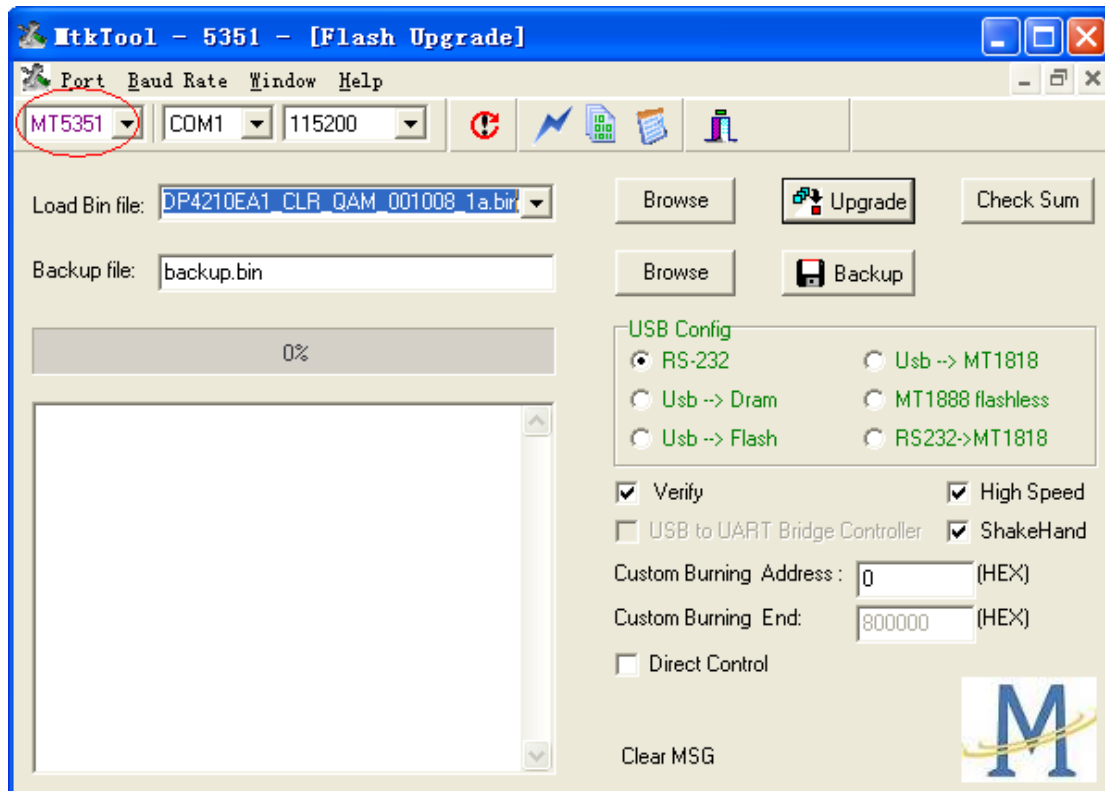
Process of update MT5351AG

Preparing :

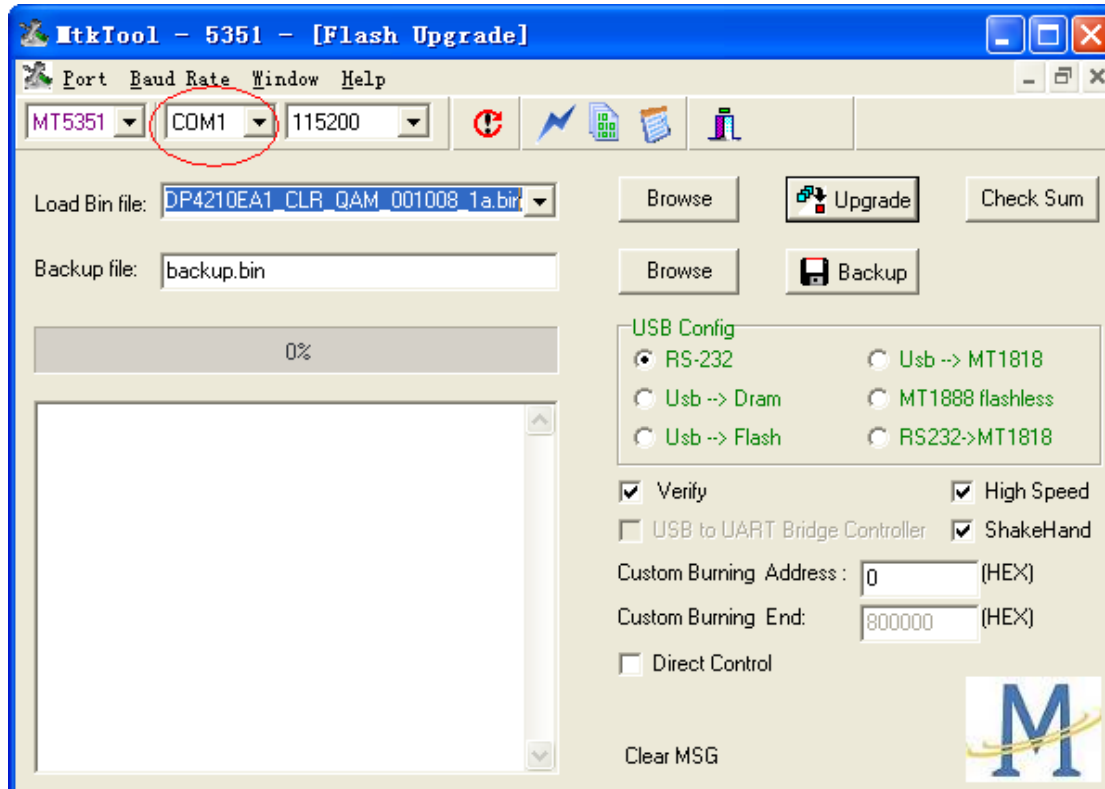
1. Connect **RS232 download line**, One connector is connected to **RS232 connect port of Plasma TV** , while another side is connected to PC COM port.
2. Store the MtkTool into the PC

Downloading :

3. Turn on AC power switch of the Plasma TV and then press the button “standby” of the remote control . The image could be found on the screen of the Plasma TV while the color of the power indicator is green . (the mode of the Plasma TV will be standby mode if after turn on the main power switch only .)
4. Execute MTKtool and select the chipset as MT5351AG. (the software of MTKtool will be sent to your side)



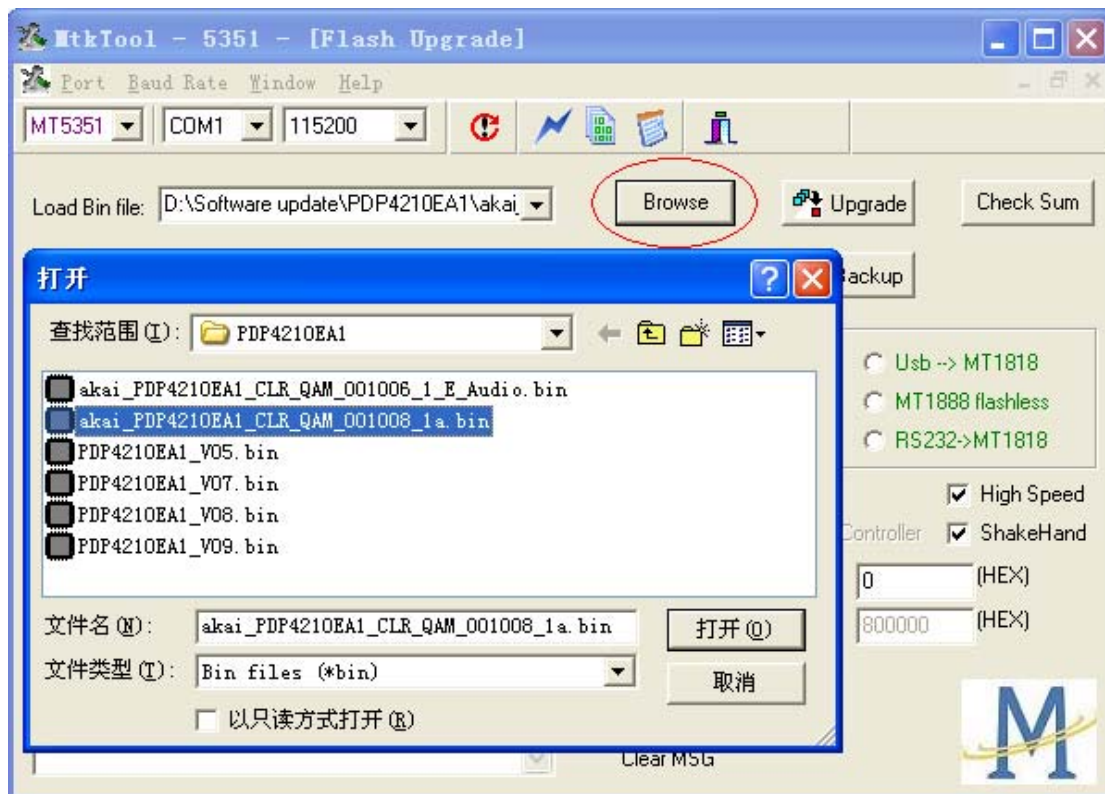
5. Select current COM port. (please try to check the COM port of your PC).



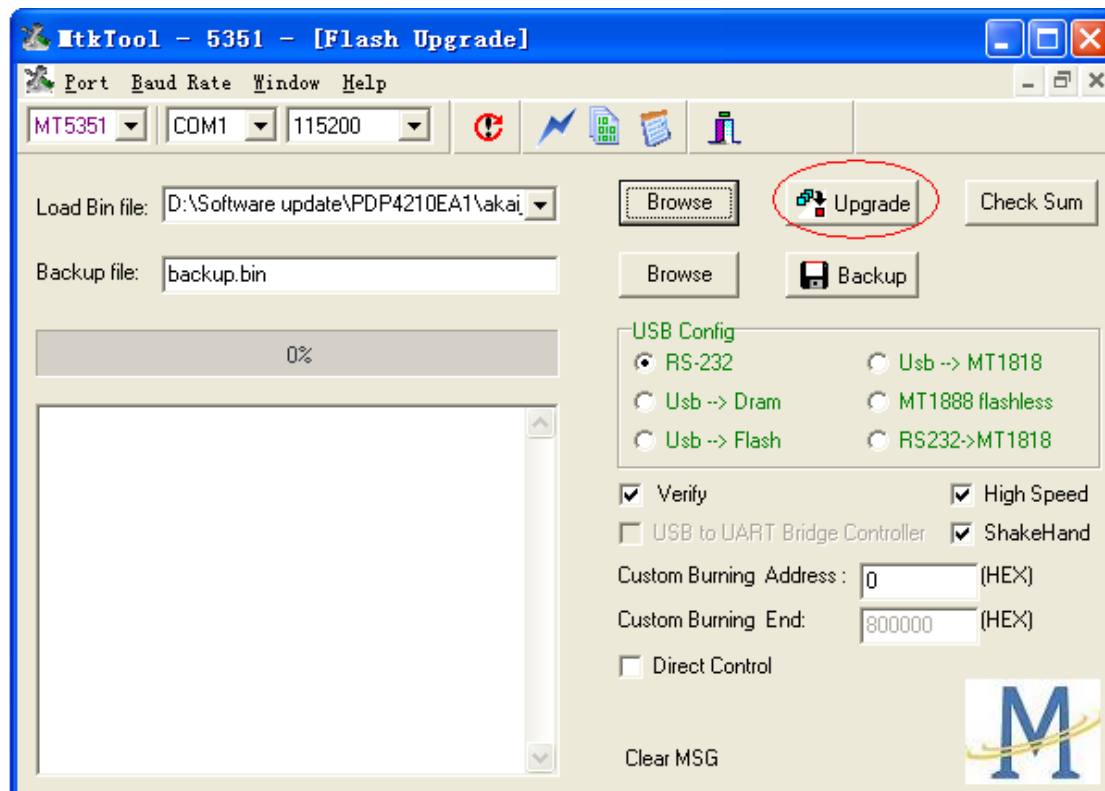
6. Choose the bit rate as 115200.

7. Select the update binary by pressing browse button. For example, the binary file name is

XXXX_PDP4210EA1_000000XX_X_P.bin. (this update firmware will be sent to your side)



8. Press Upgrade button and start update process.



9. The update process is successful as the progress bar is 100%. After the update process is ok, turn off power and wait indicator light is off. Turn on power and TV can work.

Checking :

It is needed to check the version of the firmware for MT5351AG which has been download into the Plasma TV .

Press Menu button of the remote control and the main OSD menu is appeared on the screen .

Use the remote control and select the DTV menu . following input “0000” (zero , zero , zero , zero) of the remote control .Then enter the mode of factory after input the digits .

It is easy to be found the version of the current firmware for MT5351AG is “PDP4210EA1 CLA_QAM_XXXXXX_XX”under the mode of factory .